



Accellera Continues Support for Verification and Interoperability with Formation of New Standards Committee

EDA Users Demand Interoperable Verification Components, Verification IP Committee's Goal is to Reduce Verification Costs, Improve Design Quality

Napa, Calif., May 6, 2008, — Accellera, the electronics industry organization focused on Electronic Design Automation (EDA) standards, announced today that its Board of Directors answered electronic design verification tool users' requests by approving the formation of a new verification standards committee. The **Verification Intellectual Property (VIP) Technical Subcommittee (TSC)** is chartered to define standard technology and/or methods to realize a modular, scalable and reusable generic verification environment.

Verification components and environments are currently created in different forms, making interoperability among verification tools or geographically dispersed design teams time-consuming and error-prone. The results of Accellera's VIP standardization effort will improve interoperability and reduce the cost of repurchasing and rewriting IP for each new project or electronic design automation tool, as well as make it easier to reuse verification components. Overall, the VIP standardization effort will lower verification costs and improve design quality throughout the industry.

"Accellera is addressing the electronic design industry's need for a common standard for Verification IP interoperability and reuse," remarked Shrenik Mehta, Chair of Accellera. "Our newest VIP Technical Subcommittee's goal is to improve design productivity by making it easier to verify the design components with a standardized representation that can be used with various verification tools."

About SystemVerilog and VIP

The SystemVerilog Hardware Design and Verification Language (HDVL) is a language of choice for modern design and validation. It has been standardized as IEEE 1800 and is being deployed today by users and tool vendors alike. Yet, there isn't a standard to create and use VIP

written in the SystemVerilog language. Accellera's VIP TSC will offer the next generation of benefits from SystemVerilog to verification engineers.

Why Interoperable VIP Components?

Verification solutions are ubiquitous, differing from company to company and among separate organizations within companies. Commercial tool suppliers do not support all the verification solutions in use today. The result is that there are many different methods for doing the same thing, requiring retraining and conversion costs. Interoperable VIP components reduce the cost of using and re-using VIP and improve the quality of design verification by eliminating translation errors.

Call for Participation

Accellera's VIP Technical Subcommittee is open for participation by everyone. Accellera membership brings additional benefits to participants. To contribute to the group's activities, please visit www.accellera.org/activities/vip to request to join the VIP Technical Subcommittee.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE Standards Association for formalization and ongoing change control.

For more information about Accellera, please visit www.accellera.org.

-end-

Press Contacts:

Georgia Marszalek, ValleyPR for Accellera, +1 650 345 7477, Georgia@ValleyPR.com

Notes to editors:

Acronyms

IEEE Institute of Electrical and Electronics Engineers

VIP Verification Intellectual Property

All trademarks and tradenames are the property of their respective holders.