



## **Accellera Announces New Unified Power Format Standard to Advance Low-Power Integrated Circuit Design**

*Open Standard has Foundation in Proven Technologies*

NAPA, Calif., February 28, 2007 — Accellera, the electronics industry organization focused on electronic design automation standards, announced today that its members and Board of Directors have approved the **Unified Power Format (UPF) 1.0** as an Accellera standard. The Accellera Board approval this week follows approval by Accellera's Technical Sub-Committee (TSC) last month.

The UPF standard is a convergence of proven technology donations from seven companies. EDA vendor contributions were derived from several years of successful use of their products on taped-out low-power designs. End-customers contributed their internally-developed optimization and analysis technologies which deal with application-specific power issues, especially for wireless and hand-held devices. Strong collaborative participation by Accellera members and other dedicated companies resulted in an open standard that was developed in only 5 months.

When power consumption is a key consideration, describing low-power design intent with Accellera's UPF improves the way complex integrated circuits can be designed, verified and implemented. The open standard permits all EDA tool providers to implement advanced tool features that enable the design of modern low-power ICs. Starting at the Register Transfer Level (RTL) and progressing into the detailed levels of implementation and verification, UPF facilitates an interoperable, multi-vendor tool flow and ensures consistency throughout the design process.

“Our well-established processes and excellent technical resources have made it possible for Accellera to offer yet another standard to improve design productivity in record time,” remarked Shrenik Mehta, chair of Accellera. “When leveraged in a design flow, our UPF standard will improve the efficiency and economics of how designers can optimize IC power requirements.”

A UPF specification defines how to create a supply network to supply power to each design element, how the individual supply nets behave with respect to one another, and how the logic functionality is extended to support dynamic power switching to these logic design elements. By controlling the operating voltages of each supply net and whether the supply nets (and their connected design elements) are turned on or off, the supply network only provides power at the level the functional areas of the chip need to complete the computational task in a timely manner.

“The UPF technical subcommittee experienced unprecedented cooperation among EDA competitors and end-customers,” said Stephen Bailey, UPF technical subcommittee chair. “Their diligent and focused efforts have resulted in a complete and comprehensive standard that offers a solid foundation for low power design and verification solutions.”

### **UPF Availability**

The Accellera UPF 1.0 standard specification is available now at no cost at [www.accellera.org](http://www.accellera.org).

### **About Accellera**

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. Participation in Accellera’s technical subcommittees is open to all interested companies and individuals. Membership in Accellera is encouraged, but not required, to be involved in the development of Accellera standards. As a result of Accellera’s partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed seven standards that have been ratified by the IEEE. Accellera’s recent successes in advanced design and verification standards include OCI, OVL, SystemVerilog and PSL. For more information about Accellera, please visit [www.accellera.org](http://www.accellera.org).

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### Notes to editors:

Electronic versions of UPF graphics are available on request.

An Accellera UPF supporters quotes are available at [www.accellera.org](http://www.accellera.org) in the Press Room section.

### Acronyms

IEEE Institute of Electrical and Electronics Engineers

UPF Unified Power Format

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