



Accellera Continues to Promote Increased Electronic Design Productivity with Revised VHDL Standard

Revision approval follows Accellera's approval of VHDL API specification

NAPA, Calif., Oct. 9, 2006, — Accellera, the electronics industry organization focused on electronic design automation standards, announced today that its members and Board of Directors have approved a revised version of the VHDL specification. The revision integrates the Property Specification Language (PSL), adds Intellectual Property (IP) protection methods and offers improvements that increase designer productivity.

In July, the organization announced approval of the VHDL Applications Programming Interface (API) standard known as VHPI. Both standards have been transferred to the IEEE for their consideration as revisions to the VHDL standard, IEEE Std. 1076™-2002.

Accellera's VHDL Technical Subcommittee (TSC) works with the IEEE VHDL Analysis and Standardization Group (VASG) on standardization.

"Accellera has well-established processes for delivering standards in a timely manner and transferring them to the IEEE," said Shrenik Mehta, chair of Accellera. "For VHDL, the IEEE granted us the permission to revise the language, and with the efforts of over 50 engineers representing more than 20 companies, we were able to finalize the development and approve a revised specification in less than a year."

"This revision has truly been a tag-team effort," said Jim Lewis, IEEE VASG chair.

"The IEEE VASG started the work in early 2003, and Accellera's VHDL Technical Subcommittee took over the work in 2005, funded its technical editing, and did super-human work to finalize it. We are pleased that these language extensions and productivity enhancements are standardized for industry adoption."

“Accellera’s efforts to enhance VHDL will continue,” added Lance Thompson, Accellera’s VHDL TSC Chair, “We encourage individuals and companies to join the VHDL Technical Subcommittee and Accellera to help further our work.”

What’s New-PSL, IP protection, Enhancements, Bug Fixes

The Accellera-approved VHDL standard integrates PSL, allowing PSL statements to appear in the body of VHDL description. In addition, design units were created that permit PSL files to be separate from the design. The standard adds IP protection mechanisms and supports methods that allow designers to specify what portions of the design are to be encrypted and protected, what method to employ, and the name of the key to use for decryption. Further, the standard adds facilities to make objects (usually signals) visible from within an encrypted and protected region.

Other enhancements include:

- parameterizable packages using generics to increase package reuse.
- fixed and floating point packages with generics for customization.
- hierarchical signal reference to allow testbenches to drive and read signals deep in the design.
- simplified sensitivity lists using process(all)
- composite types (records and arrays) that permit elements to be unconstrained arrays (facilitates user defined matrix types and potentially future standard matrix types).
- std_logic_vector is now a subtype of std_ulogic_vector removing the necessity for conversions.
- simplified conditionals (if, ...) that allow use of types bit and std_logic in addition to boolean.
- unary reduction operators (XOR data)
- overloading logic operators to allow mixed scalar and vector arguments
- approximately 50 corrections and clarifications to the previous revision of the language

Call for Participation

Work continues on the next revision of VHDL in the areas of object orientation, transaction level modeling, constrained random and coverage support. To participate in these areas and others, contact Lynn Horobin at lynnh@acellera.org and request to join the VHDL Technical Subcommittee.

Availability

The revised VHDL standard is available to Accellera members and Accellera VHDL Technical Subcommittee members at www.accellera.org.

About VHDL, the IEEE and Accellera

The IEEE granted Accellera permission to create derivative works and return them to the IEEE for publication. The IEEE continues to own the copyright for and is the sole publisher of VHDL. Accellera provides a framework that enables the technical work of its committees, logistics, and the infrastructure for obtaining and distributing required funds and resources.

Accellera VHDL Technical Subcommittee has over 55 technical members representing 10 member companies and numerous non-member companies. See <http://www.accellera.org/activities/vhdl> for more information.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed seven standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and PSL. For more information about Accellera, please visit www.accellera.org.

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Notes to editors:

Acronyms

IEEE Institute of Electrical and Electronics Engineers

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language

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