

**ACCELLERA APPLAUDS IEEE 1800™ SYSTEMVERILOG STANDARD APPROVAL**  
*Electronic Design Industry Backs Standard for System-on-Chip Design and Verification*

NAPA, California – November 9, 2005- Accellera, the electronics industry organization focusing on electronic design automation (EDA) standards, today welcomed the Institute of Electrical and Electronics Engineers' (IEEE) announcement that it has approved the SystemVerilog hardware description and verification language as IEEE Std.1800™-2005, "Standard for SystemVerilog Unified Hardware Design, Specification and Verification Language." The rapid approval by the IEEE through its Corporate Standards Program finalizes the accreditation process and provides design and verification engineers assurance that their SystemVerilog system-on-chip (SoC) designs are based on a single, stable standard.

"The approval process was expedited due to close cooperation among EDA tool providers, semiconductor and system companies, Accellera and the IEEE," said Shrenik Mehta, Accellera chair. "The approval of this standard is a sterling example of how an industry can work towards a common goal for the benefit of the entire design and verification community."

Thanks to the fast ratification process, EDA companies are now able to introduce even more tools that support SystemVerilog. All tool developers can feel comfortable developing products that support the full standard. To date, there are more than 75 announcements of tools and services for SystemVerilog from Accellera member companies and the industry at large. The unprecedented, rapid support the EDA industry has shown for this standard indicates a new age of improved interoperability among EDA tools.

"As one of the first EDA companies to introduce SystemVerilog tools and methodologies, Synopsys has demonstrated its dedication to bringing advanced, standards-based solutions to its customers in a timely manner," said Manoj Gandhi, senior vice president and general manager, Verification Group at Synopsys, Inc. "We're proud to have donated key technologies to the SystemVerilog standard that are already delivering productivity gains to the design community. The IEEE's approval of SystemVerilog means that users can be confident that they are backed by the IEEE's reputation for providing solid and complete standards."

As the number of EDA tools available on the market climbs, SoC engineers will reap the benefits of using SystemVerilog to increase their productivity and reduce costs of design and verification. Several SystemVerilog features improve the existing Verilog modeling techniques, including advanced design modeling capabilities, testbench constructs, verification methods using assertion and testbench language, and easier interoperability with other languages.

“Mentor is committed to SystemVerilog and is a leader in deploying SystemVerilog capabilities across its products,” said Robert Hum, Vice President and General Manager of Mentor Graphics Design Verification and Test Division. “SystemVerilog’s integration of new methodologies, like assertion-based verification and testbench automation, into a single hardware design language greatly simplifies the adoption and use of the new verification flows that designers need today. The standardization of the language coupled with the widespread support of EDA vendors ensures that designers can confidently move forward with SystemVerilog for their projects.”

SystemVerilog was developed as an extension to the widely used Verilog hardware description language. It began in Accellera with donations from Accellera member companies BlueSpec, Mentor Graphics, Motorola, Novas, Real Intent and Synopsys, as well as user-driven enhancements. It was transferred to the IEEE for ratification under its new Corporate Standards Program and took only a little more than one year to move from transfer to ratification by the IEEE. This timeline is in striking contrast to the three-to-five years that EDA standards typically used to require.

"Cadence has not only embraced but applied SystemVerilog in its mixed language Incisive and Encounter design and verification platforms. It is a core element of our recently announced Incisive Design Team and Enterprise solutions, and our suite of Encounter implementation tools," said Victor Berman, Group Director of Language Standards at Cadence Design Systems. "As the original developers of Verilog, we are very pleased to see the rapid advancement of this vastly improved version through the standardization process and are proud to have done our part in contributing to this significant industry milestone."

Standards provide value for large well-established companies, smaller emerging companies, and the user base as a whole. Looking forward, Accellera and the IEEE will continue their role as a catalyst, enhancing the rapid deployment of relevant design solutions to the market.

“As an early technology contributor and ongoing active participant in Accellera, Real Intent is proud of our role in SystemVerilog,” said Prakash Narain, President and CEO, Real Intent. “The standardization of SystemVerilog is significant due to the real gains in verification efficiency our customers are seeing. Now design teams can confidently write and prove assertions using Real Intent tools and be assured they are compatible with solutions from other vendors.”

### **About SystemVerilog**

SystemVerilog expands language-based electronic design with new and powerful design and verification capabilities, fully aligned with and built upon the Verilog-2005 standard, IEEE Std.1364™-2005. Its enhancements include the extension of memory system tasks for complex memory modeling, operator overloading for simplified expressions, and tagged unions with pattern matching for code conciseness and improved formal analysis. Assertion enhancements span environmental constraints to facilitate formal analysis and random simulation, and a broader scope of assertions for more comprehensive behavior and design intent specification. Testbench generation improvements encompass fine-grain process control for multi-threaded testbench development; dynamic and static queues with stream generation for complex verification scenarios; virtual interfaces for expressiveness of testbench infrastructure; and random weighted case plus functional coverage.

Further information about SystemVerilog can be found at [www.systemverilog.org](http://www.systemverilog.org).

### **About Accellera**

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera’s partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit [www.accellera.org](http://www.accellera.org).

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Note to editors: Please visit [www.accellera.org](http://www.accellera.org) to see a quote sheet from Accellera members and SystemVerilog supporters.

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