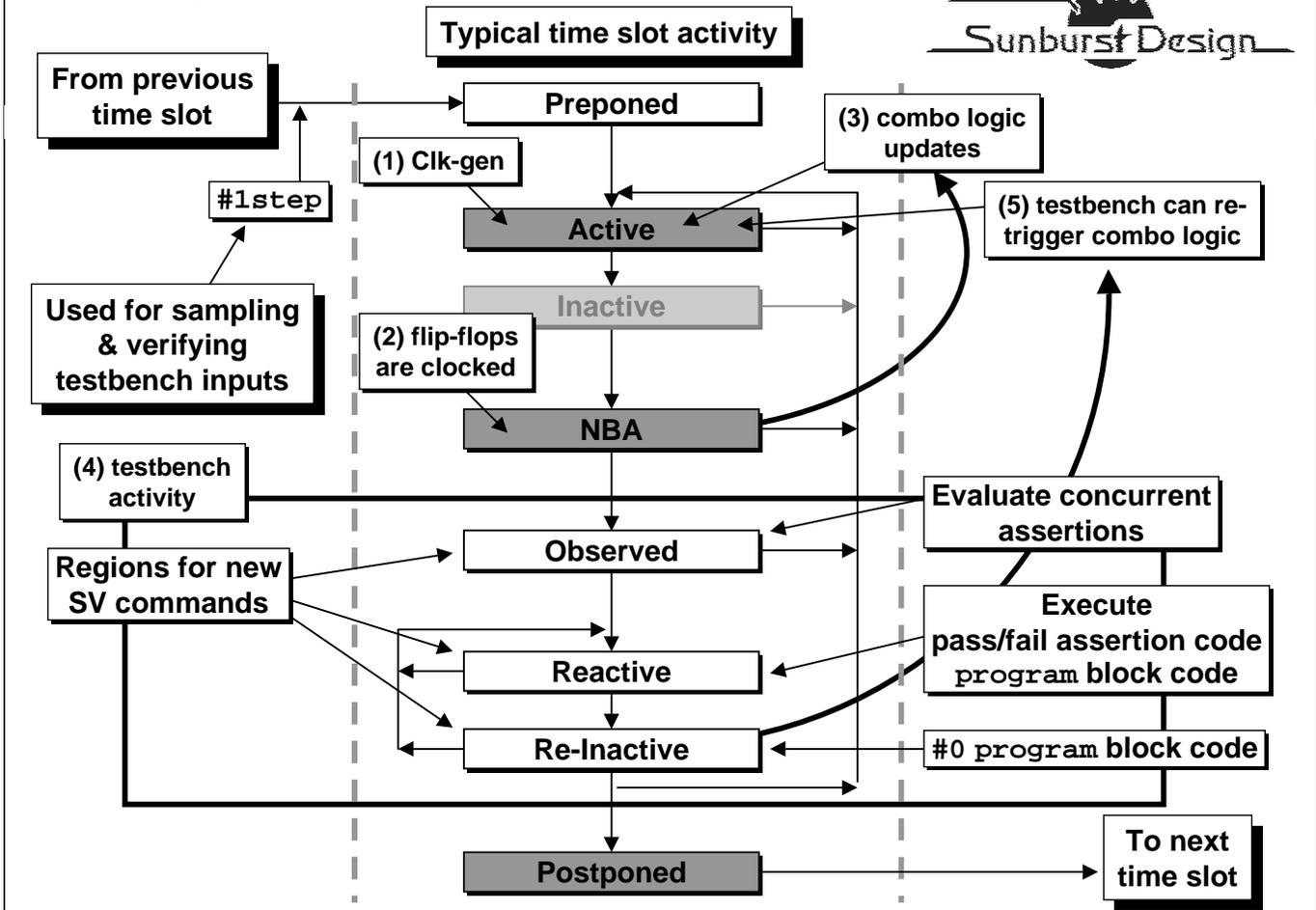## Scheduling of New SV Commands

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The Sunburst Design-preferred methodology forces stimulus generation to take place away from the active clock edge, but for engineers who want to apply stimulus on the active clock edge, putting the stimulus generation into new SystemVerilog **program** regions helps to reduce RTL-testbench race conditions, because the testbench code will not fire until the RTL code has initially responded to active clock and combinational logic activity.

Stimulus code applied on the active clock edge is really intended to trickle through the combinational logic and setup before the next active clock edge, not the clock edge in the current time slot. The **program** testbench code will potentially update the combinational logic in the same time slot before advancing time. If the clock generator is put into the **program** testbench (not recommended), the **program** code clock might not trigger properly coded RTL nonblocking assignments without a race, especially if the clock signal passes through some type of combinational clock buffer, which could delay the clocking action until after the stimulus has propagated to the inputs of the RTL flip-flops (this is an undesirable race that can be avoided by putting the clock generation into the top-level module).

It is interesting to note from the figure above, that even though most engineers think that active events happen before nonblocking assignment events, in a properly coded 0-delay RTL design, only the clock executes first in the active events region, which triggers all of the nonblocking assignment flip-flop events, which then triggers the combinational logic; hence, most nonblocking assignment events execute and complete before the combinational active events are triggered.

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