SV-EC January Face-to-Face
21 January 2003

accellera

David Smith – Chairman
Stefen Boyd – Co-Chairman

Overview

- Milestones/Schedule
- Overview of work left
- Guidelines
- Today's Agenda

Milestones
From Board Presentation

- End of January
  - Content Fix
  - SV-EC (Complete 3.1 LRM review w/o other committes)
- February 24, 2003
  - First Full LRM draft
    - Part One : Language LRM (sv-ac, sv-bc, sv-ec)
    - Part Two: C Interface LRM (sv-cc)
  - Distribute at DVCON 2003
  - Quality Gate 1
  - SV-EC (Complete 3.1 LRM)
- April 1, 2003
  - Freeze technology (Review in March/April)
  - Quality Gate 2
- May 1, 2003
  - Final draft to Accellera board
  - May used for wording clarification adjustment and cosmetic changes
  - Quality Gate 3
  - SV-EC (LRM to board)
- June 1, 2003
  - Standard Release

Schedule

Meeting Date	Milestone Date	Meeting Objective/Milestone
January 21, 2003		Review integrated LRM - Full day meeting
January 27, 2003	`	1 Hour meeting for LRM Review
	January 28, 2003	Complete Review of 3.1 LRM (without SV-CC, SV-BC, SV-ACC additions)
February 3, 2003		Review SV-CC/SV-BC/SV-AC additions to LRM
February 10, 2003		1 Hour meeting for LRM Review
February 17, 2003		US Holiday - skip meeting NEED ALTERNATE DATE
February 24, 2003		1 Hour meeting for LRM Review
	February 24, 2003	Complete 3.1 LRM
March 3, 2003		Review SV-CC/SV-BC/SV-AC additions to LRM
March 10, 2003		1 Hour meeting for LRM Review
March 17, 2003		Review SV-CC/SV-BC/SV-AC additions to LRM
March 31, 2003		Technology Freeze, only clarification and editing
April 14, 2003		Clarification and Editing of LRM
April 28, 2003		Clarification and Editing of LRM
	May 1, 2003	LRM to Accellera board
	June, 2003	System Verilog 3.1 complete

Work Left

1. Chapter 7 Operators and Expressions
   - Section 3 (increment/decrement)
   - Section 5 (Wild equality/inequality)
   - Section 10 (String concatenation)
2. Chapter 8 Procedural Statements and Control Flow
   - Section 4.2 (enhanced for loop)
   - Section 7 (Process statement)
3. Chapter 9 Processes
   - Section 1 (introduction - fork join and process control)
   - Section 6 (Dynamic Processes)
   - Section 7 (fork...join)
   - Section 9 (Process control)
4. Chapter 10 Tasks and Functions
   - Section 1 (introduction - argument enhancements)
   - Section 3.2 (discarding return values)
   - Section 4 (Task/Function scope & lifetime)
   - Section 5 (Task and Argument function passing)
5. Chapter 11 Classes *
6. Chapter 12 Inter-Process Synchronization and Communication *
7. Chapter 13 Clocking Domains *
8. Chapter 14 Signal Operations *
9. Chapter 15 Program Block *
10. Annex C String Methods
11. Annex D Linked Lists

* Major Sections
Core of testbench

Guidelines

- All of these topics have been discussed before
  - Numerous review sessions
- Presentations have been give as to why capability is provided and what it means
- Would like to focus today on new issues or resolution of existing open issues and on detailed review results
  - REV-12/REV-13/REV-14 are open issues
- Since EXT-19 Scheduling Semantics is core to Chapters 13-15 we need to discuss as well.
- Focus on technology that is defined and implemented

Today's Agenda

9:00 - 9:15 Introduction

9:15 – 10:30 Clocking Domains

10:30 – 10:45 Break

10:45 - 12:00 Signal Operations and Program Block

12:00 - 1:00 Lunch

1:00 – 1:30 Scheduling Semantics

1:30 - 2:30 IP Synch/Communication

2:30 – 2:45 Break

2:45 - 4:00 Classes