

For Release August 2, 2004

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Accellera Approves Updated Property Specification Language Standard for Electronic Design Verification, Begins IEEE Standardization Process

New Version Aligns Accellera's PSL Standard with SystemVerilog Assertions

NAPA, California—August 2, 2004 Accellera, the electronics industry organization focused on electronic design automation (EDA) standards, today announced that its Board of Directors, representing systems, semiconductor and design tool member companies, approved Accellera's **Property Specification Language (PSL) standard version 1.1** as an Accellera design verification standard last month, and that the organization has begun the IEEE standardization process for PSL with the IEEE Corporate Advisory Group (CAG).

Accellera's PSL standard addresses the shortcomings of natural language forms of design specification. It allows engineers to capture the functional specifications of logic design—in a way that is unambiguous, effective and concise—using the notion of properties and assertions. The expressiveness of PSL allows users to easily specify design behavior with properties, and document design requirements with assertions, saving time and effort in the design verification cycle.

“PSL 1.1 supports the new age of design verification,” said Dennis Brophy, Accellera Chairman. “Effectively, it takes the electronics industry into the era of assertion-based verification, a powerful means for increased confidence in the correctness of a chip or system design prior to fabrication.”

“We are very pleased to see the ratification of PSL 1.1 as the next generation of the Accellera property specification language standard,” said Erich Marschner, a Senior Architect at Cadence Design Systems and co-chair of the Accellera technical committee that defined PSL. “PSL and assertion-based verification have been recognized by many as essential for verification of today's increasingly complex designs. The completion of PSL 1.1 demonstrates that PSL will continue to grow in capability, to address increasingly challenging verification requirements.”

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What's New

The PSL 1.1 effort focused on refinement of PSL 1.01 and on alignment of syntax and semantics between PSL and SystemVerilog Assertions (SVA) where possible. In addition to correcting errata discovered in PSL 1.01, PSL 1.1 incorporates new features and user-driven enhancements that benefit EDA vendors and users alike. The PSL extensions subcommittee focused on common requests from users, including the addition of a SystemVerilog flavor, adoption of SVA built-in functions, addition of labels on directives as well as report clauses on certain directives, relaxation of some flavor macros and refinement of operator precedence.

PSL Information & LRM

For more information about PSL 1.1 or to obtain a copy of the Language Reference Manual (LRM), please visit www.accellera.org.

About Accellera

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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Acronyms

CAG - Corporate Advisory Group

EDA - Electronic Design Automation

IC - Integrated Circuit

IEEE - Institute of Electrical and Electronic Engineers

LRM – Language Reference Manual

PSL – Property Specification Language

SVA – SystemVerilog Assertion

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