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Accellera Announces Significant Improvement in Electronic Design & Verification, Approves SystemVerilog 3.1a Standard, Begins IEEE Process

NAPA, Calif., May 24, 2004, — Accellera, the electronics industry organization focused on electronic design automation (EDA) standards, today announced that its Board and Technical Committee members--systems, semiconductor and design tool companies--have approved SystemVerilog 3.1a as an Accellera standard for language-based design verification, and that the organization has begun the IEEE standardization process.

SystemVerilog evolves language-based electronic design with new and powerful design and verification capabilities, fully aligned with and built upon the Verilog-2001 standard known as IEEE Std 1364™-2001.

Now available as an Accellera standard, the SystemVerilog 3.1a Language Reference Manual (LRM) completes the work on the SystemVerilog standard after a period of feedback, testing and usage by EDA developers and early users. User feedback was a critically important part of creating version 3.1a, bringing credibility, robustness and new features to the standard. To date, more than 30 companies have announced product support, services and plans to support the SystemVerilog language.

“SystemVerilog 3.1a truly heralds the age of unified design and verification languages,” said Dennis Brophy, Accellera Chairman. “Our work on language-based design started over 10 years ago with the Verilog and VHDL hardware description language standards, and we are very pleased to announce another significant milestone in the evolution of design language standards that improves both design and verification and to be working with the IEEE-Standards Association to accelerate the accreditation of SystemVerilog 3.1a.”

“The SystemVerilog 3.1a committees have analyzed over 300 feedback items with 90% approval, indicating wide acceptance of SystemVerilog by both users and EDA vendors,” remarked Vassilios Gerousis, Accellera's Technical Committee Chairman.

Gerousis added, “Based on this community feedback, the SystemVerilog technical subcommittees focused our 3.1a release on the stability of the language and the addition of user-requested enhancements. As we did with SystemVerilog 3.0 and 3.1, we maintained complete backward compatibility with the IEEE Std 1364-2001 standard and SystemVerilog errata releases.”

What’s New

In addition to correcting errata discovered in SystemVerilog 3.1, SystemVerilog 3.1a incorporates new features and user-driven enhancements that benefit vendors and users alike. Bluespec, Mentor Graphics, Motorola, Novas Software and Synopsys donated technology, which was incorporated with earlier SystemVerilog technology donations from Real Intent and Synopsys for version 3.1.

SystemVerilog 3.1a provides many enhancements for advanced design including the extension of memory system tasks for complex memory modeling, operator overloading for simplified expressions, and tagged unions with pattern matching for code conciseness and improved formal analysis.

Assertion enhancements improve the ability of designers and verifiers to specify design intent and behavior. These include environmental constraints to facilitate formal analysis and random simulation, and a broader scope of assertions for more comprehensive behavior specification.

Enhancements for testbench generation include: fine-grain process control for multi-threaded testbench development; dynamic and static queues and stream generation for complex verification scenarios; virtual interfaces for flexibility and expressiveness of testbench infrastructure; random weighted case and functional coverage for users to set up a meaningful constrained-random environment.

Several of SystemVerilog 3.1a's features are aimed at improving the existing Verilog use model. Separate compilation and packages allow a C- or VHDL-like approach to compiling code in individual pieces. A vendor-independent API allows access of proprietary waveform file formats for higher performance and obsoletes the disk-consuming ASCII Value Change Dump (VCD) files. SystemVerilog tasks can be exported in the DPI so that a foreign language can interact with SystemVerilog as if it were interacting with its own, such as a C routine that calls a task that consumes time and blocks until that task completes.

SystemVerilog Information & Support

For more information about SystemVerilog, to obtain a copy of the Language Reference manual (LRM) or information on product support, services and plans for SystemVerilog, please visit www.accellera.org.

About Accellera

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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Acronyms

API	Application Programming Interface
DPI	Direct Programming Interface
EDA	Electronic Design Automation
HDL	Hardware Description Language
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
IEEE-SA	IEEE Standards Association
PLI	Programming Language Interface
VCD	Value Change Dump
VHDL	VHSIC (Very High-Speed IC) HDL