



Accellera Hosts Key Events and Supports Workshop at Design Automation Conference in Anaheim, California

Who

At the [Design Automation Conference](#) (DAC), [Accellera](#), the electronics industry organization focused on Electronic Design Automation (EDA) standards, is supporting a DAC Workshop covering its standards, Open Verification Library (OVL), SystemVerilog Assertions (SVA) and Property Specification Language (PSL); hosting an open industry meeting with a presentation of its 5th annual Technical Excellence Award and standards presentations covering Accellera's [standards](#), including Verilog-AMS (Analog/Mixed Signal) and the new Verification IP (VIP) Technical Subcommittee; and holding its annual DAC breakfast, sponsored by Denali, with a panel on the topic of *How to Reduce Costs, Complexity and Time to Market*.

When and Where

DAC Workshop beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL

1:00pm-5:15pm, Monday, June 9, 2008

Anaheim Convention Center Room 207D

Accellera Technical Committee Update and Technical Excellence Award Presentation

11:00am - 12:00pm, Tuesday, June 10, 2008

DAC Exhibitor Forum, Exhibit Hall D (Booth 2849)

Accellera Breakfast and Panel Discussion, Sponsored by Denali

7:30am - 9:30am, Wednesday, June 11, 2008

Anaheim Convention Center Room 303D

Topic: "Save Money Now! How to Reduce Costs, Complexity and Time to Market"

More about the Accellera Events at DAC

[DAC Workshop beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL](#)

Organizer and Speaker:

Harry Foster, Chief Verification Technologist, Mentor Graphics Corporation, Addison, TX, USA

Mr. Foster is also Chair of Accellera Formal Verification Technical Committee, Technical Advisor to the Accellera Open Verification Committee and Chair of the IEEE 1850 PSL Working Group.

Speakers:

Mike Turpin, ARM Ltd., Cambridge, UK

Erik Seligman, Intel Corporation, Hillsboro, OR, USA

Mercedes Tan, Sun Microsystems, Santa Clara, CA, USA

Sivan Rabinovich, IBM, Haifa, Israel

Joe Richards, Broadcom Inc., Santa Clara, CA, USA

This is a DAC workshop. Please register at www.dac.com.

[Accellera Technical Committee Update and Technical Excellence Award](#)

Accellera will present its current standards activities including progress on Verilog-AMS and the new Verification IP technical committee. The recipient of the 2008 Technical Excellence Award will also be presented with the award in recognition of contributions to the development of standards. Presenters include Accellera Chairman, Shrenik Mehta of Sun Microsystems, Accellera Technical Committee Chair, Karen Pieper of Tabula and representatives of Accellera Technical Subcommittees.

This event is open to all DAC Exhibition attendees. To register for DAC, please visit www.dac.com.

[Accellera Breakfast and Panel Discussion, Sponsored by Denali](#)

Topic: "Save Money Now! How to Reduce Costs, Complexity and Time to Market"

Abstract:

Today's competitive consumer-driven markets demand feature-rich capabilities to ensure market success. With the rising demand for new, higher-performance applications based on new technologies, manufacturers face increasing bill-of-materials (BOM) costs. Clearly, there must be some new ways to reduce material costs. When designing many portable-systems, what are new ways to integrate functionality and achieve their cost and footprint goals? A handful of industry luminaries will examine the complexity and costs related to front-end design and verification compared to manufacturing in this SoC era.

Organizer, David Lin, Denali

Moderator: Charles DeLisio, D-Side Advisors

Karen Pieper, Accellera Technical Committee Chair

Robert Blake, Altera

Ted Vucurevich, Cadence Design Systems

Bob Piece, Denali

Kaveh Massoudian, IBM

This event is *free* to DAC attendees but you must register. [Reserve your seat here.](#)

Information

For more information about Accellera and Accellera standards, please visit www.accelera.org.

About Accellera

[Accellera](#) provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

For more information about Accellera, please visit www.accelera.org.

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