



Accellera Supports VHDL 4.0 Standard and IEEE 1076™-2008 Ratification

San Jose, Calif., DVCon, February 20, 2008, — Accellera, the electronics industry organization focused on Electronic Design Automation (EDA) standards, announced today that its members and Board of Directors have approved the VHDL 4.0 standard specification. VHDL 4.0 is a refinement of VHDL 3.0 (approved by Accellera in October 2006) based on feedback from trial implementations. Accellera has immediate plans to release VHDL 4.0 to the IEEE for balloting in 2008 and to support the IEEE 1076™-2008 balloting process.

VHDL 4.0 addresses over 90 issues that were discovered during the trial implementation period for the VHDL 3.0 version. These encompass enhancements to major new areas introduced by VHDL 3.0 including generic types, Intellectual Property (IP) protection, Property Specification Language (PSL) integration, VHPI (VHDL Application Programming Interface (API)) integration, and the introduction of fixed and floating point types.

“We have established an effective process for delivering standards in a timely manner and transferring them to the IEEE,” said Shrenik Mehta, chairman of Accellera. “The IEEE gave us permission to revise the VHDL language and continue to improve it, thereby addressing the needs of the VHDL community.”

Jim Lewis, chair of the VHDL Analysis and Standards Group (VASG), added, “The VASG has plans in place to bring Accellera’s VHDL 4.0 to IEEE for balloting as IEEE 1076-2008. We are pleased that these VHDL language extensions and productivity enhancements are being standardized for industry adoption with Accellera’s support.”

“Accellera’s efforts to enhance VHDL are continuing,” remarked Lance Thompson, Accellera’s VHDL Technical Subcommittee (TSC) Chair. “Over the past 18 months, Aldec, Cadence Design Systems and Mentor Graphics have created trial implementations, which have helped us clarify the documentation in the areas that were introduced in VHDL 3.0. In addition, we’ve also incorporated issues resolved by the VASG’s Issues Screening and Analysis Committee (ISAC).”

A copy of Accellera’s October 2006 VHDL 3.0 news release is at www.accellera.org/pressroom/2006/AccelleraVHDL100906.pdf.

Call for Participation

To participate in Accellera’s VHDL efforts, please contact Lynn Horobin at lynnh@accellera.org and request to join the VHDL Technical Subcommittee.

Availability

The VHDL 4.0 standard is available to Accellera members and Accellera VHDL Technical Subcommittee members at www.accellera.org.

About VHDL, the IEEE, and Accellera

Accellera’s VHDL Technical Subcommittee (TSC) works with the IEEE VASG on standardization. The IEEE granted Accellera permission to create derivative works and return them to the IEEE for publication. The IEEE continues to own the copyright for and is the sole publisher of VHDL.

Accellera provides a framework that enables the technical work of its committees, logistics, and the infrastructure for obtaining and distributing required funds and resources. Accellera’s VHDL TSC has over 80 technical members including representatives from nine Accellera member companies. See <http://www.accellera.org/activities/vhdl> for more information.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

For more information about Accellera, please visit www.accelera.org.

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Notes to editors:

Acronyms

IEEE Institute of Electrical and Electronics Engineers

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language

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