



Accellera Announces Election of Officers for 2008/9

*Shrenik Mehta, Chair; Dennis Brophy, Vice-Chair;
Karen Bartleson, Secretary; Yatin Trivedi, Treasurer*

NAPA, Calif., October 28, 2008 — Accellera, the electronics industry organization focused on Electronic Design Automation (EDA) standards, announced today that its Board of Directors elected officers for its 2008/9 membership year earlier this month.

Shrenik Mehta, Senior Director, Frontend Technologies & OpenSPARC program, Microelectronics, Sun Microsystems, was re-elected Chair. Dennis Brophy, Director of Strategic Business Development, Mentor Graphics, was re-elected Vice-Chair. Karen Bartleson, Senior Director, Interoperability, Synopsys, was elected Secretary, and Yatin Trivedi, Senior Director, Strategic Alliances, Magma Design Automation was elected Treasurer.

"Accellera continues to be a very significant player in developing EDA standards that improve electronic design productivity," remarked Shrenik Mehta, Accellera chair. "I am again honored to be elected chair for a fourth term and to be part of the group that defines and delivers electronic design standards that benefit the global electronics industry."

Accellera Member companies for 2008/9 are listed at <http://www.accellera.org/join/roster>. Accellera provides a framework that enables the technical work of its committees, logistics and the infrastructure for obtaining and distributing funds and resources for EDA standards that, when approved, are available to everyone in the electronics community at no cost.

About Accellera's Electronic Design Standards

Accellera has transferred its completed standards work to the IEEE and continues to use this strategy as part of the roadmap for all of its standards.

To date, seven Accellera EDA standards have been ratified by the IEEE – Hardware Description Language (HDL) standards, Verilog or IEEE 1364, VHDL or IEEE1076, Property Specification Language (PSL) or IEEE 1850 and SystemVerilog or IEEE 1800; Standard Delay Format (SDF) or IEEE 1497; Delay and Power Calculation System (DPCS) or IEEE 1481 and Advanced Library Format (ALF) or IEEE 1603. In addition, two standards are active in IEEE working groups: Open Compression Interface (OCI) or IEEE 1718 and Unified Power Format (UPF) or IEEE P1801. Accellera's most recent IEEE advanced design and verification language standards include the SystemVerilog and PSL standards.

About Accellera's Technical Subcommittees

Accellera's Technical Subcommittees produce effective and efficient standards for today's advanced IC designs. Participation comes from Accellera member companies, industry contributors, and independents. Technical contributors typically have many years of practical experience with IC design and developing and using design automation tools.

Accellera's [Technical Subcommittees](#) include: Interface (ITC), Open Compression Interface (OCI), Open Verification Language (OVL), Property Specification Standard (PSL), SystemVerilog, Unified Coverage Interoperability (UCI), Unified Power Format (UPF), Verilog Analog/Mixed-Signal (Verilog-AMS), Verification Intellectual Property (VIP) and VHDL. More information is at www.accellera.org.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE Standards Association for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

-end-

Press Contact:

Georgia Marszalek, ValleyPR for Accellera, +1 650 345 7477, Georgia@ValleyPR.com

Notes to editors:

Photos are available on request and more information about Accellera's Officers can be found by visiting their LinkedIn profiles.

Shrenik Mehta: <http://www.linkedin.com/in/shrenikm>
Dennis Brophy: <http://www.linkedin.com/in/dennisbrophy>
Karen Bartleson: <http://www.linkedin.com/in/karenbartleson>
Yatin Trivedi: <http://www.linkedin.com/in/yatintrivedi>

Acronyms and Abbreviations

ALF Advanced Library Format
AMS Analog, Mixed Signal
DPCS Delay and Power Calculation System
EDA Electronic Design Automation
HDL Hardware Description Language
IC Integrated Circuit
IEEE Institute of Electrical and Electronics Engineers
OCI Open Compression Interface
PSL Property Specification Language
SDF Standard Delay Format
Std. Standard
UPF Unified Power Format
VHDL Very High-Speed IC (VHSIC) HDL

All trademarks and tradenames are the property of their respective holders.