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Accellera Board Approves New Version of Analog, Mixed-Signal Standard

*Standard unifies Verilog HDL standard IEEE Std. 1364 with Accellera's AMS standard,
Results in easier implementations by tool developers and more efficient top-down verification*

Napa, Calif., August 20, 2008, — [Accellera](#), the electronics industry organization focused on Electronic Design Automation (EDA) standards, announced today that its Board of Directors and Technical Committee members – systems, semiconductor and design tool companies – approved a new version of its Verilog-Analog Mixed-Signal (AMS) standard, **Verilog-AMS 2.3**, as an Accellera standard for analog and mixed-signal design and simulation. The new Verilog-AMS standard unifies the Verilog-AMS 2.2 specification with the IEEE Std. 1364™-2005 or Verilog hardware description language (HDL) standard.

Verilog-AMS 2.3 enables users to develop standard and tightly integrated Verilog-AMS modules and allows EDA software tool developers to implement EDA tools without ambiguities in the language interpretation.

Verilog-AMS 2.3 encompasses analog and mixed-signal extensions to IEEE Std. 1364, which is widely used today for digital circuit design and verification. The previous Accellera Verilog-AMS standard, [Verilog-AMS 2.2](#), was approved in 2005.

“The Verilog-AMS 2.3 language release is an important milestone for our Technical Committee and the industry at large,” said Shrenik Mehta, Accellera chairman. “A unified Verilog-AMS language integrated with the IEEE Verilog standard improves AMS design and will result in an increased acceptance of the standard.”

"Accellera's AMS standard is a reality due to the enormous efforts of our Subcommittee members, who are driven by the goal to improve the productivity of AMS designers and the quality of mixed-

signal designs," added Sri Chandrasekaran, Accellera's Verilog-AMS Technical Subcommittee chairman.

More about the New Accellera AMS standard

Apart from IEEE-1364 integration, Verilog-AMS 2.3 introduces new analog and mixed-signal features to support and enable improved top-down AMS design and verification methodologies. These include enhancements to table_model, support for multiple analog blocks, and resolution of language conflicts with the SystemVerilog IEEE Std. P1800, such as, changing the digital domain name to 'ddiscrete' from 'logic' as logic is a keyword in SystemVerilog, and making the usage of array literals consistent.

The next phase of Accellera's AMS technical activities will include integration of the AMS standard with the SystemVerilog language, IEEE Std. P1800, and extensions to the AMS language for mixed-signal assertions and behavioral modeling support.

To participate in the Accellera AMS Technical Sub-Committee efforts, please visit www.accellera.org/activities/verilog-ams/.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE Standards Association for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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Press Contacts:

Georgia Marszalek, ValleyPR for Accellera, +1 650 345 7477, Georgia@ValleyPR.com

Notes to editors:

Acronyms and Abbreviations

AMS	Analog, Mixed Signal
EDA	Electronic Design Automation
HDL	Hardware Description Language
IEEE	Institute of Electrical and Electronics Engineers
Std.	Standard

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