



Accellera's UPF (Unified Power Format) Featured at 19th EDA

Interoperability Developers' Forum

Thursday, April 26, 2007 in Santa Clara, California

Who:

Accellera, the Electronic Design Automation (EDA) organization focused on electronic design standards, invites the electronic design community to learn more about Accellera's newest standard, the Unified Power Format (UPF), at the free Low Power session during the 19th EDA Interoperability Developers' Forum.

What:

Low Power Session Features UPF Technical Tutorial and Panel Discussion

How will low power designs be defined, verified and implemented? What should EDA vendors know about UPF (Unified Power Format)? Come learn more about Accellera's UPF that serves the entire low power design flow. The session features a technical tutorial on UPF, plus a panel discussion, "Scaling the Power Wall."

Speakers:

Karen Bartleson, Accellera

Anand K. Iyer, ArchPro Design Automation

Kevin Kranen, Synopsys

Alan Ma, Mentor Graphics

Arvind Narayanan, Magma Design Automation

Jim Sproch, Synospys

Yatin Trivedi, Magma Design Automation

When/Where:

19th EDA Interoperability Developers' Forum

Thursday, April 26, 2007, 9:30AM – 11:45AM

Sun Microsystems Conference Center at Agnews Historic Park

4030 George Sellon Circle

Santa Clara, CA 95054

Information

To register, at no cost, for the Power of One session, and for more information on the EDA Interoperability Developers' Forum, please visit

<http://synopsys.com/news/events/devforums/2007/apr/index.html>

About UPF

When power consumption is a key consideration, describing low-power design intent with UPF improves the way complex integrated circuits can be designed, verified and implemented. The open standard permits all EDA tool providers to implement advanced tool features that enable the design of low-power ICs. Starting at the Register Transfer Level (RTL) and progressing into the detailed levels of implementation and verification, UPF facilitates an interoperable, multi-vendor tool flow and ensures consistency throughout the design process. The UPF specification is publicly available at www.accellera.org.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE for formalization and ongoing change control.

Accellera has developed seven standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). Accellera is currently developing another new standard, the Unified Coverage Interoperability (UCIS) standard.

For more information about Accellera, please visit www.accellera.org.

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