



Accellera Invites DAC Attendees to Open Meetings and Events

June 4-7, San Diego Convention Center, San Diego, California

Who

This year Accellera, the Electronic Design Automation (EDA) organization focused on design standards, is once again hosting a variety of events at the Design Automation Conference (DAC), and inviting the EDA community to attend its open meetings and events as well as Conference's Low Power Workshop.

What, When and Where

Accellera Open Industry / Membership Meeting

Wednesday June 6, 2007

10:00am-11:30am Convention Center Room 27A

Accellera Technical Committees will provide standards updates and honor the recipient of Accellera's Technical Excellence Award. This meeting is open to all DAC attendees.

Accellera Breakfast and Panel Discussion:

Panel Topic: "Design: The Next Frontier for SystemVerilog"

Wednesday June 6 2007

7:30am-9:30am, Convention Center Room 26AB

The industry asked for SystemVerilog, and Accellera delivered! Panelists representing commercial IP providers, EDA vendors, and IP consumers will address real world benefits of SystemVerilog in the design domain, and examine state-of-the art flows for SoC design, which is next frontier for SystemVerilog. The panel and breakfast are sponsored by Denali Software, and are open to all DAC attendees.

Moderator: Gary Smith - GarySmithEDA

Panelists: Gary Delp - LSI Logic

Marc Greenberg – Denali Software

Robert Papp - Intel

Dave Rich - Mentor Graphics

Bryan Bullis - Cisco

Birds of a Feather Session- Unified Coverage Interoperability

Wednesday June 6, 6:30pm-8:30pm, Convention Center

Accellera members plan to organize DAC "Birds of a Feather" sessions to discuss the Unified Coverage Interoperability (UCI) standard. Accellera's UCI Technical Subcommittee (TSC) is charged with defining standards to enable sharing and analysis of coverage data generated by different tools during the verification process. Sign-up sheets will be available in the DAC registration area and the meeting will be assigned a room if enough attendees register at the show.

Unified Power Format (UPF) Booth # 7860

UPF, the Unified Power Format standard from Accellera, enables open, multi-vendor tool flows and solutions for low-power design. Accellera is one of the sponsors of the UPF booth at DAC where UPF will be demonstrated in products from a range of EDA suppliers who support the UPF standard.

Expert Speakers at the UPF Booth:

Anand Iyer, ArchPro: Are You Sure Your Power Management Scheme Works?

Rob Aitken, ARM: Library Considerations for Low Power

David Allen, Atrenta: Atrenta Support of UPF

Edward Rashba, IEEE: Leveraging the Standards Lifecycle at IEEE

Juergen Karmann, Infineon: UPF - New Potentials for a Low Power Design Flow

Gary Delp, LSI: A Comparison of Power Aware Design Intent Formats

Ed Huijbregts, Magma: Multivoltage Domain Issues

Stephen Bailey, Mentor: UPF by Example

Michael Keating, Synopsys: UPF - Challenges of a Paradigm Shift

Jim Sproch, Synopsys: Exploring UPF's Capabilities

Mary Ann White, Virage: Silicon-Proven Low Power Semiconductor IP Overview

Karen Bartleson, Accellera: Open, Fast, Inclusive: Doing a Standard the Right Way

DAC Workshop: Design and Verification of Low Power ICs

Sunday June 3, 2007

4:00pm-7:00pm. Convention Center Room 6E

For more information, visit

<http://www2.dac.com/data2/44th/44AcceptedPapers.nsf/0/D4E8466857C8D63E872572A4006F0593>.

Information & Registration

For more information about Accellera and Accellera standards, please visit www.accellera.org

To register for Accellera's open meetings and events, please visit

<http://www.accellera.org/events/>.

For more information about DAC and to register for the Low Power Workshop, please visit

www.dac.com.

About Accellera's Technical Excellence Award and Technical Subcommittees

Each year, Accellera's Technical Excellence Award recognizes the outstanding achievements of its Technical Subcommittee members. Candidates are nominated by the industry at large, and nominations are endorsed by participants in Accellera's Technical Subcommittees. All Accellera Technical Subcommittee members are eligible for the award.

Accellera's Technical Subcommittees include Interface, Open Compression Interface (OCI), Open Verification Language (OVL), Property Specification Standard (PSL), SystemVerilog, Unified Coverage Interoperability (OCI), Unified Power Format (UPF), Verilog Analog Mixed-Signal (Verilog-AMS) and VHDL.

Accellera's Technical Subcommittees produce effective and efficient standards for today's advanced IC designs. Participation comes from Accellera member companies, industry contributors, and independents. Technical contributors typically have many years of practical experience with IC design and developing and using design automation tools.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

Accellera has developed seven standards that have been ratified by the IEEE. Accellera's successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). Accellera recently completed the Unified Power Format (UPF) standard and is currently developing a Unified Coverage Interoperability (UCI) standard.

For more information about Accellera, please visit www.accellera.org.

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