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Accellera Approves Functional Design Verification Standard

OVL 2.0 Improves Electronic Design Quality,

Supports Assertion-Based Verification with Verilog, VHDL, SystemVerilog and PSL

NAPA, Calif., August 23, 2007, — Accellera, the electronics industry organization focused on Electronic Design Automation (EDA) standards announced today that its Board of Directors, representing semiconductor, Intellectual Property (IP), EDA companies and systems houses, approved Accellera's Open Verification Library (OVL) 2.0 as an Accellera verification standard last month. OVL improves electronic design quality and supports Assertion-Based Verification (ABV) with Verilog, SystemVerilog, VHDL and the Property Specification Language (PSL).

The Accellera OVL standard includes a library of assertion checkers provided as an open standard. It improves electronic design verification when using Hardware Description Languages (HDLs) and results in better quality designs by enabling effective use of ABV methodologies.

“Our Open Verification Library 2.0 standard is an open source version of assertion checkers, allowing reuse in various verification environments,” said Shrenik Mehta, Accellera Chair. “The open standard is part of a growing series of Accellera's evolving electronic design language standards, like SystemVerilog and PSL that improve verification and design quality by enabling powerful verification methodologies.”

What's New

“OVL has been used for five years as a vendor-neutral and language-independent assertion methodology to functionally verify designs in simulation and formal verification environments. OVL version 2.0 represents a major step forward for users, while still being fully backwards compatible with earlier versions,” said Mike Turpin, Accellera OVL technical subcommittee chair.

“A powerful new feature in OVL is the ability to synthesize assertions into emulators, accelerators and FPGA prototyping environments, extending assertion-based verification with OVL to support the full verification flow, with simulation, formal verification, hardware-assisted verification and FPGA prototyping,” added Kenneth E. Larsen, Accellera OVL technical subcommittee co-chair.

Version 2.0 adds synthesizable checkers that include “enable” and “fire” ports for additional control of the checkers when used in hardware flows including emulation, FPGA prototyping or ASIC error detection. There are also 17 new and more advanced checkers, taking OVL to a total of 50 assertion checkers that cover many of the common properties that engineers check during functional verification. There is now a VHDL implementation of the 10 most popular checkers, and finer control of X checking on a per-instance basis. Version 2.0 is backward compatible with previous versions of Accellera OVL.

About Accellera’s OVL Effort

Accellera OVL technical committee was formed in early 2005 and the first OVL standard was announced in August 2005. In addition to creating more checkers and maintaining the standard the committee plans to add features and welcomes new members and contributions.

OVL Availability

The Accellera Standard OVL 2.0 standard is available now for download at the Accellera website: www.accellera.org.

More information and examples are available at a users’ site: www.eda-stds.org/ovl.

About Accellera Standards

Accellera has developed nine standards that have been transferred to the IEEE. Seven have been ratified by the IEEE and the two newest ones are in active IEEE working groups now.

Accellera’s successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL).

About Accellera's Technical Subcommittees

Accellera's Technical Subcommittees produce effective and efficient standards for today's advanced IC designs. Participation comes from Accellera member companies and independent industry contributors. Technical contributors typically have many years of practical experience with IC design and developing and using design automation tools.

Accellera's current Technical Subcommittees include: Interface (ITC), Open Compression Interface (OCI), Open Verification Language (OVL), Property Specification Standard (PSL), SystemVerilog, Unified Coverage Interoperability (UCI), Unified Power Format (UPF) ,Verilog Analog/Mixed-Signal (Verilog-AMS) and VHDL. More information is at www.accellera.org.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

For more information about Accellera, please visit www.accellera.org.

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