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## **Accellera Announces Election of Officers**

*Shrenik Mehta, Chair; Dennis Brophy, Vice-Chair;  
Karen Bartleson, Treasurer; Stanley J. Krolikoski, Secretary*

NAPA, Calif., October 22, 2007 — Accellera, the electronics industry organization focused on Electronic Design Automation (EDA) standards, announced today that its Board of Directors elected officers for its 2007/8 membership year last month.

Shrenik Mehta, Senior Director, Frontend Technologies & OpenSPARC program, Microelectronics, Sun Microsystems, was re-elected Chair. Dennis Brophy, Director of Strategic Business Development, Mentor Graphics, was re-elected Vice-Chair. Karen Bartleson, Director of Interoperability, Synopsys, was elected Treasurer, and Stanley J. Krolikoski, Ph.D. Group Director, Standards and Interoperability, Cadence Design Systems, was elected Secretary.

"Accellera is a significant player in developing new EDA standards that improve electronic design productivity," said Shrenik Mehta, Accellera chair. "I am again honored to be elected chair for a third term and to be part of the group that continues to define and deliver standards that benefit the global electronics industry."

Accellera Corporate Member companies for 2007/8 are: [ARM Ltd.](#), [Cadence Design Systems](#), Denali Software, [Freescale Semiconductor](#), [IBM](#), [Intel Corporation](#), [Magma Design Automation](#), [Mentor Graphics](#), [Nokia](#), [Novas](#), [Rockwell Collins](#), [Sun Microsystems](#), [Synopsys Inc.](#) and [Texas Instruments](#).

## **About Accellera's Electronic Design Standards**

Accellera has transferred its completed standards work to the IEEE and continues to use this strategy as part of the roadmap for all of its standards.

To date, seven Accellera EDA standards have been ratified by the IEEE – Hardware Description Language (HDL) standards, Verilog or IEEE 1364, VHDL or IEEE1076, Property Specification Language (PSL) or IEEE 1850 and SystemVerilog or IEEE 1800; Standard Delay Format (SDF) or IEEE 1497; Delay and Power Calculation System (DPCS) or IEEE 1481 and Advanced Library Format (ALF) or IEEE 1603. In addition, two standards are active in IEEE working groups, Open Compression Interface (OCI) or IEEE 1718, and Unified Power Format (UPF) or IEEE P1801. Accellera's most recent advanced design and verification language standards include the SystemVerilog and the Property Specification Language (PSL) standards.

## **About Accellera's Technical Subcommittees**

Accellera's Technical Subcommittees produce effective and efficient standards for today's advanced IC designs. Participation comes from Accellera member companies and independent industry contributors. Technical contributors typically have many years of practical experience with IC design and developing and using design automation tools.

Accellera's current Technical Subcommittees include: Interface (ITC), Open Compression Interface (OCI), Open Verification Language (OVL), Property Specification Standard (PSL), SystemVerilog, Unified Coverage Interoperability (UCI), Unified Power Format (UPF), Verilog Analog/Mixed-Signal (Verilog-AMS) and VHDL. More information is at [www.accellera.org](http://www.accellera.org).

## **About Accellera**

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

For more information about Accellera, please visit [www.accellera.org](http://www.accellera.org).

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