



**Accellera's Vice Chairman, Dennis Brophy, to Present at the SystemVerilog
User Forum at EDS Fair**

Friday, January 26, 13:30-15:30, Pacifico Yokohama, Japan

Who/What

Accellera, the Electronic Design Automation (EDA) organization focused on electronic design standards, invites the electronic design community in Japan to attend the SystemVerilog User Forum at the Electronic Design and Solution (EDS) Fair to hear from Accellera's Vice-Chairman, Dennis Brophy, about market adoption and support of SystemVerilog, a hardware design, specification and verification language standard (also known as IEEE Std.1800™) and work within the IEEE on the creation of the next SystemVerilog standard.

When/Where

Friday, January 26, 13:30-15:30 (Mr. Brophy will be speaking at 13:30.)

Pacifico Yokohama

Exhibition Hall, Annex Hall

1-1-1, Minato Mirai

Nishi-ku, Yokohama 220-0012

Information

For more information about Accellera and its EDA standards please visit www.accellera.org.

For more information on EDS Fair, please visit www.edsfair.com.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

Accellera has developed seven standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). Accellera is currently developing a Unified Power Format (UPF) and Unified Coverage Interoperability (UCIS) standard.

For more information about Accellera, please visit www.accellera.org.

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