

**Call for Registrations, Accellera Hosts a Free Power Lunch with
Interoperable EDA Tool Demonstrations
and a VHDL Tutorial with the IEEE at DATE**

Tuesday, April 17th, Nice, France

Who:

Accellera, the Electronic Design Automation (EDA) organization focused on electronic design standards, invites the electronic design community to attend its free Power Luncheon , and its VHDL Tutorial, co-sponsored with the IEEE, at the Design Automation and Test Conference (DATE).

What:

UPF Luncheon and Workshop with Interoperable Tools Demonstrations

How will you define, verify and implement your next low power design? Join Mentor Graphics, Synopsys and Magma for an educational luncheon seminar and demonstrations of EDA tools that support Accellera's UPF standard. See how it extends logic design specifications with low power information such as isolation and retention strategies, power domain definition, supply distribution and switching for verification and implementation.

VHDL Tutorial

Learn the new features introduced in the Accellera VHDL standard 3.0, its new fixed-point and floating-point packages, and a look into the next set of revisions being worked on in committee.

Speakers:

Dennis Brophy, Accellera Vice Chairman

Edward Rashba, IEEE, New Business Ventures

Jim Lewis, SynthWorks, VHDL Expert, and Chairman of the IEEE VHDL Analysis and Standardization Group (VASG)

When/Where:

UPF Luncheon and Workshop

Tuesday 17th April, noon - 3 p.m.

Novotel, Matisse/Chagall Conference Room

Nice, France

VHDL Tutorial

Tuesday 17th April, 3 p.m. - 6 p.m.

Gallieni 4, Acropolis

Nice, France

Information

To register for the Accellera sessions, please visit <http://www.accellera.org/events/>

For more information about Accellera and its EDA standards please visit www.accellera.org.

For more information on DATE, please visit www.date-conference.com.

About UPF

When power consumption is a key consideration, describing low-power design intent with UPF improves the way complex integrated circuits can be designed, verified and implemented. The open standard permits all EDA tool providers to implement advanced tool features that enable the design of low-power ICs. Starting at the Register Transfer Level (RTL) and progressing into the detailed levels of implementation and verification, UPF facilitates an interoperable, multi-vendor tool flow and ensures consistency throughout the design process.

What's New in VHDL

Accellera's VHDL Technical Subcommittee (TSC) works with the IEEE VHDL Analysis and Standardization Group (VASG) on standardization. Accellera VHDL standard 3.0, approved in July of last year, includes the VHDL Applications Programming Interface (VHPI), PSL (integrated into VHDL), IP protection, fixed-point and floating-point packages, as well numerous improvements to the language. These improvements include enhancements to generics, composite types, case statements, conditional expressions, sensitivity lists, and hierarchical signal reference.

About the IEEE Standards Association

The IEEE Standards Association, a globally recognized standards-setting body, develops voluntary consensus standards through an open process that brings diverse parts of an industry and the public together. These standards set specifications and procedures based on current scientific consensus. The IEEE-SA has a portfolio of some 900 active standards and more than 400 standards in development. For information on the IEEE-SA see: <http://standards.ieee.org/>.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

Accellera has developed seven standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). Accellera is currently developing a Unified Power Format (UPF) and Unified Coverage Interoperability (UCIS) standard.

For more information about Accellera, please visit www.accellera.org.

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