

Stephen Bailey to Receive Accellera's 2007 Technical Excellence Award at DAC

Award Recognizes Bailey's Leadership of the Unified Power Format Standard

NAPA, Calif., May 30, 2007 — Accellera, the electronics industry organization focused on electronic design automation standards, has selected **Stephen Bailey** as the 2007 recipient of its 4th annual Technical Excellence Award for his commitment to leading the Unified Power Format (UPF) standard from inception to its successful completion. The Award will be presented at Accellera's Open Industry meeting during the Design Automation Conference (DAC), Wednesday, June 6, 2007, 10:00-11:30am, San Diego Convention Center, Room 27A. To attend this meeting, please register at <http://www.accellera.org/events>.

“Stephen Bailey, our UPF Technical Subcommittee chair, led us to the completion of an Accellera standard in record time, all the while working to gain broad industry support and adoption,” said Shrenik Mehta, Accellera chairman. “He inspired the best from the committee he led, and his efforts raised the bar to a new height in terms of technical achievement for Accellera.”

An open standard for low-power design was requested by users at DAC in 2006, and was approved by the Accellera Board of Directors as a standard in February of this year. Strong, collaborative participation by Accellera members and other dedicated companies resulted in an open standard that was developed in only 5 months. Seven companies donated proven technology to Accellera, and the UPF technical subcommittee converged them into a single standard under Mr. Bailey's leadership.

The standard enables EDA tool interoperability for designing power applications, especially for wireless and hand-held devices where power management is a critical factor. It is publicly available for download at no charge at <http://www.accellera.org>.

The UPF standard will be explained in Accellera's workshop, “Design and Verification of Low Power ICs,” at DAC on Sunday, June 3, 2007, 4:00-7:00pm, San Diego Convention Center, Room 6E. Mr. Bailey will be among the experts presenting example-based usage of UPF and demonstrations of EDA tool support for the standard.

When power consumption is a key consideration in IC design, describing low-power design intent with Accellera's UPF improves the way complex integrated circuits can be designed, verified, and implemented. The open standard permits all EDA tool providers to implement advanced tool features

that enable the design of modern low-power ICs. Starting at the Register Transfer Level (RTL) and progressing into the detailed levels of implementation and verification, UPF facilitates an interoperable, multi-vendor tool flow and ensures consistency throughout the design process. Engineers who design low-power ICs are the ultimate beneficiaries of the exceptional accomplishments of Mr. Bailey's Subcommittee.

About Stephen Bailey

Stephen Bailey is the product marketing manager for Questa in the Design for Verification and Test group at Mentor Graphics. He has been part of the EDA industry for over 15 years, and his career has provided the opportunity to experience virtually all facets of electronic design. Mr. Bailey has served in several industry standards activities including VHDL IEEE 1076 working group chair, Property Specification Language (PSL) IEEE 1850 working group member, IEEE Design Automation Standards Committee secretary, Accellera Unified Power Format Technical Subcommittee chair, and Accellera Unified Coverage Interoperability Standard Technical Subcommittee member.

About Accellera's Technical Excellence Award and Technical Subcommittees

Each year, Accellera's Technical Excellence Award recognizes the outstanding achievements of its Technical Subcommittee members. Candidates are nominated by the industry at large, and nominations are endorsed by participants in Accellera's Technical Subcommittees. All Accellera Technical Subcommittee members are eligible for the award.

Accellera's Technical Subcommittees include Interface, Open Compression Interface (OCI), Open Verification Language (OVL), Property Specification Standard (PSL), SystemVerilog, Unified Coverage Interoperability (OCI), Unified Power Format (UPF), Verilog Analog Mixed-Signal (Verilog-AMS) and VHDL.

Accellera's Technical Subcommittees produce effective and efficient standards for today's advanced IC designs. Participation comes from Accellera member companies, industry contributors, and independents. Technical contributors typically have many years of practical experience with IC design and developing and using design automation tools.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership

with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

Accellera has developed seven standards that have been ratified by the IEEE. Accellera's successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). Accellera recently completed the Unified Power Format (UPF) standard and is currently developing a Unified Coverage Interoperability (UCI) standard.

For more information about Accellera, please visit www.accellera.org.

-End-

Press Contact:

Georgia Marszalek, ValleyPR for Accellera, +650 345 7477, Georgia@ValleyPR.com

Notes to editors: A photo of Stephen Bailey is available on request.

All trademarks and tradenames are the property of their respective holders.