

For Immediate Release

Accellera Approves High Performance Electronic Design Verification Standard

Co-Emulation Modeling Interface Standard Adds Significant Enhancements

NAPA, California—May 11, 2007-- Accellera, the electronics industry organization focused on electronic design automation (EDA) standards, today announced that its Board of Directors, representing systems, semiconductor and design tool member companies, approved Accellera's **Standard Co-Emulation Modeling Interface (SCE-MI) 2.0** specification as an Accellera verification standard. A previous version of the standard, SCE-MI 1.1, was approved by the Accellera Board in April 2005. The work on the standard was done by Accellera's Interface Technical Committee (ITC).

"SCE-MI 2.0 provides an easy way to connect and migrate transactor models between simulation, emulation and rapid prototyping environments," noted Accellera Chair, Shrenik Mehta. "With it, SoC design and verification teams are seeing improved electronic design productivity, and the new SCE-MI standard makes it more worthwhile for developers to support SCE-MI-based models."

"We are pleased to see the acceptance of the SCE-MI 2.0 draft specification," added Brian Bailey, Chair of Accellera's Interface Technical Committee (ITC). "Vendors are now working on their implementations which will provide additional capabilities for faster and more effective testbenches with hardware assisted solutions. We will continue to look for ways in which we can enhance the performance and usability of multi-tool verification solutions."

What's New

SCE-MI 2.0 adds a new use-model built on a subset of the SystemVerilog Direct Programming Interface (DPI) for future convergence, and it is now compatible with the Open SystemC Initiative (OSCI) Transactor Level Modeling (TLM) definition.

The new Accellera standard maintains backward compatibility with the previous version. It also has added improvements such as a streaming interface with data shaping to optimize emulation speed, increased options for model migration from simulation to emulation and vice versa, as well as more simplified transactor modeling.

Overall, these enhancements improve designer productivity and model portability for transaction-level verification on heterogeneous platforms.

About SCE-MI

The SCE-MI standard improves high speed transaction-level verification between different hardware and software simulation and emulation systems. To support designers and encourage continued adoption, it improves model portability between different verification acceleration tools.

Plans/Next Steps

In the near term, a working example will be released for using the standard and dealing with any portability issues that surface during vendor implementation. The ITC committee will also work on broadening the specification to include additional languages and constructs to stay ahead of the increasing challenges in functional verification.

About the ITC Committee & Specification

The charter of the ITC is to identify and standardize multi-abstraction and multi-domain interfaces that enable complete, high performance verification environments. Additional information about the committee can be found at www.accellera.org with pointers to links to where the latest version of the specification can be downloaded.

Accellera's Technical Subcommittees produce effective and efficient standards for today's advanced semiconductor designs. Participation comes from Accellera member companies, industry contributors and independents. Technical contributors typically have many years of practical experience developing and using design automation tools.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control.

Accellera has developed seven standards that have been ratified by the IEEE. Accellera's successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). Accellera recently completed the Unified Power Format (UPF) standard and is currently developing a Unified Coverage Interoperability (UCI) standard.

For more information about Accellera, please visit www.accellera.org.

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