

Advisory

Accellera's Open Compression Interface Technical Subcommittee Holds Session at International Test Conference

Session covers how interoperability among test logic insertion, pattern generation and diagnostic tools is possible when using on-chip scan compression

Thursday, October 26, 2:00-3:30pm, Santa Clara Convention Center, Santa Clara, California

Who/What:

At the International Test Conference (ITC), Accellera's Open Compression Interface Technical Subcommittee (OCI-TSC) will hold a session on Accellera's new OCI standard. Accellera's OCI-TSC Chair, Bruce Cory will speak about the OCI standard development work and how interoperability among tools such as test logic insertion, pattern generation and diagnosis is possible when using on-chip scan compression. Accellera is an electronics industry organization focused on language-based design and verification standards.

When: Thursday October 26, 2-3:30pm, Emerging Standards Lecture

Where: Lecture 4.3 in Ballroom D, Santa Clara Convention Center, 5001 Great America Parkway, Santa Clara, California

About Accellera's OCI standard:

OCI standardizes the interface between different suppliers' tools to enable vendor interoperability for test pattern generation and diagnosis.

Before on-chip scan compression, it was possible to use different EDA tool vendors for test pattern generation and diagnosis. On-chip scan compression changed that model because each tool supplier offers a different type of scan compression logic and a tool-specific way to pass information between the insertion, generation and diagnosis steps. OCI standardizes how data is passed from logic insertion to pattern generation and from pattern generation to diagnosis to enable designers to use different supplier tools for each step independent of the on-chip scan compression logic.

The OCI-TSC plans for OCI to become an extension to the IEEE 1450.6 standard, the Standard Test Interface Language (STIL). OCI leverages IEEE 1450.6, which is the latest extension to STIL called Core Test Language (CTL), which allows STIL to support core-based design testing. The OCI standard is available at www.accellera.org.

Registration and Information:

For more information about the ITC, please visit <http://www.itctestweek.org/>.

For more information about Accellera, please visit www.accellera.org.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed eight standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). For more information about Accellera, please visit www.accellera.org.

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