

Accellera Offers Analog, Mixed-Signal Panel at GSPx; Session Covers Design, Verification and How Standards Improve Productivity

Wednesday, November 1, Santa Clara Convention Center

Who:

Accellera, the electronics industry organization focused on language-based design standards, invites the industry to its GSPx 2006 panel on using standards to improve the design and verification productivity of Analog and Mixed-Signal design teams.

When: Wednesday, November 1, 1:00-1:45pm

Where: Exhibition Theatre, GSPx, Santa Clara Convention Center, Santa Clara, California

Registration and Information:

The session is open to all interested parties.

For more information and to register for GSPx please visit <http://www.accellera.org/events/> or www.gspx.com.

About the Panel:

Title:

Complex mixed-signal design: Can an Analog/Mixed-Signal (AMS) language standard bridge the Chasm?

Abstract:

Digital system designers are used to manipulating blocks (like processor cores and memories) at a very high-level of abstraction. But analog designers are typically used to manipulating voltages and waveforms — sometimes transistor-by-transistor. Complex mixed-signal ICs demand tight functional integration between the analog and digital parts of the signal processing chain. How do we bridge the gap between the hand-crafting used for analog and the digital block manipulation?

Accellera believes that — at the very least — AMS standards can create placeholders for the design and verification information engineers need to integrate analog and digital circuitry. The forms this information will take, the vehicles which store and deliver it, the infrastructure required to support it will be the subject of this informative and far-reaching panel. Look for the different bridges – the tools, methodologies and standards -- that will alleviate and simplify the tasks of mixed-signal design and verification teams; or will they?

Moderator: Stephan Ohr, Director of Research, Analog Semiconductors, Gartner
Panelists: Jonathan David, Scintera, Inc.

Arpad Muranyi, Intel
Dave Rich, Mentor
David Sharrit, Tiburon
Mark Gogolewski, Denali

Organizers: Sri Chandra, Freescale; Yatin Trivedi, Magma Design Automation

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed eight standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). For more information about Accellera, please visit www.accellera.org.

-end-

Press Contact:

Georgia Marszalek, ValleyPR for Accellera, (650) 345-7477, Georgia@ValleyPR.com