

## **Advisory**

### **For Immediate Release**

# **ACCELLERA ANNOUNCES FORMATION OF UNIFIED POWER FORMAT STANDARDS COMMITTEE, INVITES ELECTRONICS INDUSTRY TO PARTICIPATE**

**Who:** Accellera, an electronics industry organization that drives worldwide development and use of standards required by systems, semiconductor and design tools companies, which enhance a language-based design automation process

**What:** Invites all interested parties to participate in and contribute to its new technical subcommittee to produce a standards solution for describing low-power design intent. The Unified Power Format Technical Subcommittee (UPF-TSC) is chaired by Stephen Bailey, at [stephen\\_bailey@mentor.com](mailto:stephen_bailey@mentor.com).

All contributions and donations will be accepted and considered for inclusion in the standard. Technology donations are made using Accellera's standard donation agreement which has been used by many companies, end-customers as well as vendors, over the years.

**When:** The first meeting of the UPF-TSC will be on September 13, 2006, starting at 8:30 am PDT. Details are posted on [www.accellera.org](http://www.accellera.org). This meeting is in support of and preparation for the upcoming Low Power Workshop scheduled for October 5, 2006 to be held jointly by Si2 and Accellera.

#### **Where:**

George Sellon Circle Auditorium  
4030 George Sellon Circle, Bldg. SCA03  
Santa Clara, CA 95054

For more information, please visit [www.accellera.org](http://www.accellera.org) or contact the UPF-TSC chair,

**About the Unified Power Format:** A group of leading companies interested in low power design standards met at the Design Automation Conference in July, 2006. The result was a demand for a standard that is open, inclusive, and quick. The electronics industry will benefit from being able to describe power-aware design information in a unified format that is portable across all tools in a design flow. Design and verification engineers will save time and costs while reducing error by using a unified power format.

Accellera, in cooperation with Si2, responded by forming the UPF-TSC. The standard produced by the UPF-TSC will address the needs of design and verification engineers who face power management challenges in today's complex designs. Participation in Accellera's Unified Power Format subcommittee is open to all interested companies and individuals. Membership in Accellera is encouraged, but not required, to participate in the development of the standard.

The UPF-TSC will leverage Accellera's existing proven processes. The goal of the UPF-TSC is to prepare a standard for Accellera approval by the end of 2006. The standard will then be transferred to the IEEE-SA corporate standards program for IEEE ratification as has been done with seven other standards in the last 10 years through active cooperation between Accellera and the IEEE.

### **About Collaboration with Si2**

In the continuing collaboration with Si2, the Accellera UPF-TSC chair, along with other members of the UPF-TSC, will participate in a Joint Architecture Group to oversee the technical consistency across inter-related flows/standards spanning both groups.

### **About Accellera**

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed seven standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and PSL. For more information about Accellera, please visit [www.accellera.org](http://www.accellera.org).

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### Notes to editors:

#### Acronyms

UPF-TSC – Unified Power Format Technical Subcommittee

Si2 – Silicon Integration Initiative

IEEE – Institute of Electrical and Electronics Engineers

IEEE-SA - Institute of Electrical and Electronics Engineers Standards Association

EDA – Electronic Design Automation

PSL – Property Specification Language

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