

Si2 and Accellera Announce Low Power Standards Workshop

October 5, SEMI Headquarters, San Jose, California

Who:

Accellera, the electronics industry organization focused on language-based design standards, and the Silicon Integration Initiative (Si2), an organization focused on improving the way integrated circuits are designed and manufactured invite the industry to a Low Power Standards Workshop.

When: Thursday, October 5, 2006, 8:30am – 5:30pm

Where: SEMI Headquarters, 3081 Zanker Road, San Jose, CA, 95134

Registration and Information:

The Workshop is open to all interested parties. There is no entry fee. For more information visit http://www.accellera.org/events/Low_Power_Workshop.pdf. To register, please send an email to wbayer@si2.org

For more information and to register, please visit or send an email to wbayer@si2.org.

About the Workshop:

Low power design has been identified as a critical area for design flow improvement in the 65nm processes and beyond. This workshop, lasting a day, is intended to serve as an open forum for key contributors from EDA and end-user companies to identify the critical needs in the area of low power design, verification, and analysis of integrated circuit chips. The goal is to first assimilate requirements from a varied group of presenters from end-user design companies representing requirements to satisfy the needs of microprocessor, SoC and AMS (analog, mixed signal) chip designs. Subsequent discussions will be held among the participants at the workshop to enlist the work content and responsibilities, and to identify the specific areas (language extensions, library standards, design constraints, flow interfaces, etc.) where standards need to be created or extended to enable an open environment for more advanced low power design flows and capabilities.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the

IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed eight standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and the Property Specification Language (PSL). For more information about Accellera, please visit www.accellera.org.

About Si2

Si2 is an organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on improving the way integrated circuits are designed and manufactured in order to speed time-to-market, reduce costs, and meet the challenges of sub-micron design. Si2 is uniquely positioned to enable collaboration through a strong implementation focus driven by its member companies. Si2 focuses on developing practical technology solutions to industry challenges. Si2 represents over 100 companies involved in all parts of the silicon supply chain throughout the world. For more information about OpenAccess and Si2, visit www.si2.org.

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