

Accellera Co-Sponsors JEITA Meeting & Lunch during EDS Fair in Japan; Accellera Vice-Chair, Dennis Brophy, Speaks on SystemVerilog Plans

Friday, January 27th, Pacifico, Yokohama, Japan

Who

Accellera, the Electronic Design Automation (EDA) organization focused on language-based design standards, invites the electronic design community to attend the Japan Electronic & Information Technology Association's (JEITA) System Design Forum, held during EDS Fair and co-sponsored by Accellera and its member companies.

At the event, Accellera's vice-chairman, Dennis Brophy, will speak about Accellera's plans for the SystemVerilog unified hardware design, specification and verification language standard, also known as IEEE Std.1800™-2005. Mentor Graphics, an Accellera corporate member, is sponsoring the event's luncheon.

What

JEITA's System Design Forum 2006 Conference at EDSFair 2006 SystemVerilog session includes 3 SystemVerilog speakers:

1. SystemVerilog Standardization Report & Future Plans - Dennis Brophy, vice-chairman, Accellera
2. SystemVerilog Assertions Tutorial - Sugie-san, JEITA SystemVerilog Task Group (SV-TG) member from Zuken
3. Verilog vs. SystemVerilog for Design - Yui-san, JEITA SV-TG member from Oki Network LSI

When/What/Where:

Time/Date: 10 am - 3:30 pm, Friday, January 27, 2006

Location: Annex Hall, Pacifico Yokohama (www.pacifico.co.jp/index_e.html)

Information and Registration

Please visit <http://www.edsfair.com> for more information, and to register.

For more information about Accellera and Accellera standards, please visit www.accellera.org.

About SystemVerilog

SystemVerilog expands language-based electronic design with new and powerful design and verification capabilities, fully aligned with and built upon the Verilog-2005 standard, IEEE Std.1364™-2005. Its enhancements include the extension of memory system tasks for complex

memory modeling, operator overloading for simplified expressions, and tagged unions with pattern matching for code conciseness and improved formal analysis. Assertion enhancements span environmental constraints to facilitate formal analysis and random simulation, and a broader scope of assertions for more comprehensive behavior and design intent specification. Testbench generation improvements encompass fine-grain process control for multi-threaded testbench development; dynamic and static queues with stream generation for complex verification scenarios; virtual interfaces for expressiveness of testbench infrastructure; and random weighted case plus functional coverage.

Further information about SystemVerilog can be found at www.systemverilog.org.

About Accellera

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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