

Accellera Invites DAC Attendees to Open Meetings, Events and Design Automation Conference SystemVerilog Tutorial

- *Open Meeting Covers Accellera's Standards Roadmap*
- *SystemVerilog, VHDL and OVL Sessions Planned*
- *SystemVerilog Users speak at Wednesday, June 26 breakfast panel*

Who

This year Accellera, the Electronic Design Automation (EDA) organization focused on language-based design standards, is once again hosting a variety of events at the Design Automation Conference (DAC), and inviting the EDA community to attend its open meetings, events and DAC tutorial. Meetings topics will cover Accellera standards as well as focus on SystemVerilog, VHDL and Accellera's Open Verification Library (OVL).

What, When and Where

Open Accellera Meeting

Accellera Technical Committees will provide standards' updates and honor the recipient of Accellera's Technical Excellence Award.

Wednesday July 26, 2006 from 10:00am -11:30am, Marriott Hotel, Golden Gate Room B2

Accellera Breakfast and Panel

Topic: Mission Possible III: SystemVerilog in Action!

SystemVerilog is widely in use to increase design and verification performance, productivity and quality with broad vendor support and user adoption gaining momentum. This panel offers the opportunity to hear from users about their experiences working with SystemVerilog. There will be ample time to interact with panelists, so come prepared with your questions.

Wednesday July 26, 2006 - 7:30am - 9:30am, Marriott Hotel, Golden Gate Room A1

Moderator: Peggy Aycinena, editor EDA Confidential

Panelists: John Goodenough, ARM
Mike Burns, Freescale
Matt Maidment, Intel
Thomas Thatcher, Sun
Somdipta Roy, Texas Instruments

Open Verification Library (OVL) Technical Committee Meeting

Wednesday July 26, 2006 from 1:30pm - 3:30pm, Marriott Hotel, Golden Gate Room B2

VHDL Technical Committee Meeting

Wednesday July 26, 2006 from 3:30pm - 5:30pm, Marriott Hotel, Golden Gate Room B2

Birds of a Feather Sessions

Accellera members plan to organize DAC "Birds of a Feather" sessions for VHDL and OVL. Sign-up sheets will be available in the DAC registration lobby area and the meetings will be assigned a room by DAC if enough attendees register at the show.

Wednesday July 26 from 6:30pm-8:30pm, Moscone Convention Center

SystemVerilog DAC Tutorial

SystemVerilog: Language Tutorial and Industrial Verification Experience

Friday, July 28, 2006 from 9:00am - 5:00pm, Moscone Convention Center Room 307

Information & Registration

For more information about Accellera and Accellera standards, please visit www.accellera.org

To register for Accellera's open meetings and events, please visit

<http://www.accellera.org/events/register/>

For more information about DAC and to register for Accellera's tutorial at DAC, please visit www.dac.com.

About Accellera

Accellera provides design and verification standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. Over the years, Accellera has developed seven standards that have been ratified by the IEEE. Accellera's recent successes in advanced design and verification language standards include SystemVerilog and PSL. For more information about Accellera, please visit www.accellera.org.

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Press Contact: Georgia Marszalek, ValleyPR for Accellera, + (650) 345-7477,
Georgia@ValleyPR.com

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