



**Additional Quotes for November 9, 2005 Accellera Press Release:
Accellera Applauds IEEE 1800™ SystemVerilog Standard Approval**

Accellera Corporate Members:

Magma Design Automation

“We commend Accellera for its efforts to create a standard and promote SystemVerilog. Magma is pleased to see the continued evolution of HDLs for system-level designs and is committed to support the synthesizable subset of SystemVerilog for design implementation.”

*--Yatin Trivedi, Director, Product Marketing, Logic Design Business Unit,
Magma Design Automation*

Novas Software

“All of us at Novas are delighted that the SystemVerilog standard has been fully ratified, and we extend our appreciation and congratulations to all who labored to achieve this important milestone. The semiconductor and EDA industries will benefit greatly from this large step forward in design and verification language standardization. We have enjoyed working closely with Accellera, its committees, and our partners on SystemVerilog. Our debug and analysis products and our technical team fully support the language and are ready to go as users adopt it.”

-- Scott Sandler, CEO, Novas Software

Accellera Associate Members:

Bluespec, Inc.

“As a contributor to the SystemVerilog design language, Bluespec is enthusiastic for its standardization within IEEE. Bluespec has delivered the only ESL synthesis toolset for both control logic and datapaths by building on the syntax of SystemVerilog.”

-- Shiv Tasker, CEO, Bluespec, Inc.

JEITA

“The Electronic Design Automation Technical Committee (EDA-TC) of Japan Electronics & Information Technology Industries Association (JEITA) established a SystemVerilog Task Group, under its EDA Technical Committee, to promote standardization of SystemVerilog in Japan. This standardization of SystemVerilog IEEE Std. 1800-2005 has an important meaning to Japan's Electronics and Information Technology Industries. With the enlargement and complexity of LSI, further improvement of design productivity and quality is required. We believe that SystemVerilog will bring about solutions to such problems.”

*-- Yoshio Okamura, Chairman, Electronic Design Automation Technical
Committee (EDA-TC), Japan Electronics & Information Technology Industries
Association (JEITA)*

Companies Throughout Industry:

Ace Verification

“The standardization of SystemVerilog provides the industry with a solution which integrates the key constructs from HDLs, HVLs and Assertion languages; having these capabilities in a single standard will promote better reuse and boost industry productivity.”

-- *Akiva Michelson, CTO, Ace Verification*

Blue Pearl Software

“Blue Pearl Software is strongly committed to support the IEEE 1800 SystemVerilog standard and congratulates Accellera on achieving the IEEE ratification which is extremely helpful in focusing our engineering development activities towards a single language.”

-- *Bill Alexander, VP Marketing, Blue Pearl Software*

ComputerBasedEducation

“SystemVerilog is the next logical step in the evolution of the Verilog language. The enhancements are great and can't be ignored for any SOC designs or verifications. Having one language for design and verification brings all members of a team under one roof. The consistency leads to less errors and greater code reuse.

“The additions for synthesis added to SystemVerilog allow for a greater confidence in the output from synthesis. ComputerBasedEducation has available a self-paced online class for SystemVerilog. The class comes with approximately 100 working lab/examples that you can keep.”

-- *Jay Tyer, President, ComputerBasedEducation*

Denali Software, Inc.

“Not only is Denali supporting SystemVerilog for its PureSpec verification IP products, but we have also committed to the use of SystemVerilog in the development of our Databahn IP and Blueprint ESL tools. IEEE standardization of SystemVerilog is clearly the result of a concerted effort from dedicated people throughout the industry; it enables a whole new level of interoperability and reuse by addressing things like assertions, DPI, verification constructs, and encryption. This is definitely a memorable milestone for our industry.”

-- *Sean Smith, Chief Verification Architect, Denali Software, Inc.*

Doulos

“Doulos congratulates Accellera on the completion of the IEEE P1800 SystemVerilog standardization process. The Doulos team has worked closely over many months with its EDA partners to ensure the SystemVerilog training classes in the Doulos portfolio are tuned to the new standard and the most recent tool capabilities. The full scope Comprehensive SystemVerilog training class is now scheduled in major locations in the US and Europe, and Modular SystemVerilog is available worldwide for team-based training tailored to specific customer context. Also brand new publications in the Doulos Golden Reference Guides series covering SystemVerilog and its application are slated for early 2006.”

-- *Doulos Ltd.*

HDL Design House

“Leveraging on experience with HVL, Verilog/VHDL verification and advanced verifications methodologies (assertion based, constrained random, coverage driven), SystemVerilog comes as a natural evolving step for HDL Design House in its mission to bridge the gap in between ever increasing design complexity and time to market demands of its customers.

“With improved SystemVerilog support by EDA companies and growing community of users, SystemVerilog is a language of choice for further developments of both verification and design IPs. HDL Design House positions itself as an early adopter of unified approach of new HDVL and its methodologies.

“HVC500SV is first in a line of SystemVerilog-based solutions. It's a fully OCP2.0 compliant monitor/checker as SVA properties. SystemVerilog verification solutions for other standard interfaces: AMBA (AHB, APB), I2C, SATA are being developed.”

-- Predrag Markovic, CEO, HDL Design House

Interra Systems

“Interra Systems offers EDA tool vendors with a significant time to market value by deploying most robust front-end and comprehensive validation environment for SystemVerilog and other HDL standards. Cheetah-SV, the SystemVerilog front-end is currently in use by EDA companies to ship their SystemVerilog solutions. Beacon-SV, the SystemVerilog test suite from Interra Systems is a must have pre shipment validation criteria. Interra Systems is working continually to keep Cheetah-SV and Beacon-SV updated with latest SystemVerilog standards. More than 50 EDA companies have licensed HDL technology from Interra Systems.”

-- Interra Systems, Inc.

Jasper Design Automation

“Jasper is seeing high interest in its formal verification technology, and support for the SystemVerilog Assertions (SVA) standard is contributing to this trend. The IEEE standardization of SVA will serve to drive the adoption of formal techniques and will provide an easy migration path from simulation assertions to full formal verification of high-level requirements written in SVA.”

-- Craig Cochran, vice president of marketing, Jasper Design Automation

LOA Technology

“Being able to use one language for both design and verification, and to have that language build on the Verilog 2001 standard, makes SystemVerilog the natural choice for our SV-ATE product. The ability to integrate current ATE customer designs in Verilog with our SystemVerilog-based ATE verification environment is a big win.”

-- Al Czamara, VP HW, LOA Technology, Inc.

NoBug

“SystemVerilog enables NoBug to integrate advanced verification solutions earlier in the chip development cycle which enables a smoother path to tapeout and significant productivity gains. Standardization of SystemVerilog allows NoBug to support the development and reuse methodology with productivity enhancement tools, such as automatic translation that greatly reduce costs of migration from legacy test benches and

verification IPs to SystemVerilog. The standard thus enables a lower threshold for aligning the IP assets and legacy test benches with the advanced tool support and methodology that SystemVerilog provides.”

-- Ionel Simionescu, R&D Manager, NoBug

nSys

“As one of the leaders in Verification IP, nSys is committed to strengthening the ecosystem for SystemVerilog by providing its nVS (nSys Verification Suite) family of Verification IPs in SystemVerilog.”

-- Atul Bhatia, Director, nSys

Paradigm Works

“As a member of a growing list of developers of SystemVerilog solutions, Paradigm Works can now deliver cost effective SystemVerilog solutions based on a single, stable SystemVerilog standard. The design and verification community can now be confident that the solutions adopted will work efficiently across a wider spectrum of projects, tools and environments than was feasible earlier.”

-- Ambar Sarkar, SystemVerilog Architect at Paradigm Works

Perftrends

“SystemVerilog assertions helped us to check all PCI express checklists, targeting different layers with ease, without disturbing the RTL design.”

-- E. Magesh, Project Manager, Perftrends

PSI-Electronics & MU-Electronics

“As recognized services providers in Verification domain, both PSI-Electronics and MU-Electronics are welcoming with great interest SystemVerilog as a new IEEE standard. Our customers will now benefit from state-of-the-art verification methodology independently of the tools they use.

“PSI-Electronics and MU-Electronics have always followed up-to-date evolutions in verification and EDA development and are ready to provide customers with the state-of-the-art expertise in what is now a standard. SystemVerilog is not only a language which combines design, system and verification constructs; it's becoming the standard work base of all major new developments in both design and verification.”

-- Philippe Tauvel, General Manager, PSI-Electronics and MU-Electronics

-- Vincent Bonzom, Technical Manager, PSI-Electronics

-- Mohamad Chehadi, Technical Manager of MU-Electronics

-- Francois Cerisier, Verification Activity Leader, PSI-Electronics

Sequence Design

“We are adding SystemVerilog support to PowerTheater, our power analysis and optimization platform, to support major customers, and we are pleased to back Accellera's efforts to improve industry productivity on large designs through this new standard.”

-- Tom Miller, Vice President, Power Analysis Products, Sequence Design

Silicon Interfaces

“We welcome the adoption of a single description language for Verification and Design and smooth transitioning by the Accellera group from Functional testing to Formal Verification, based on Assertions and compliance Checkers as we ratify the standards and find it in line with our plans for our roll out plans for SystemVerilog based IPs and Verification IPs.”

-- *Subhas Basu, CEO, Silicon Interfaces*

SiMantis

“The development of SystemVerilog is a significant step forward in addressing the design and verification challenges presented by two competing priorities: increasing design complexities vs. reducing time-to-market deadlines. Given that our continued success as a leading design services company relies on our expertise in best-in-class tools and methodologies, we see SystemVerilog expertise as the next logical addition to our expanding portfolio of services and have made the necessary preparations to meet our clients' demands on this front.”

-- *Sasan Iman, President, SiMantis Inc.*

Sunburst Design

“Sunburst Design recognizes that SystemVerilog will enhance, transform and accelerate design and verification environments more than any other tool introduced in the past decade.

“If you were a SystemVerilog user a year ago, you were an early adopter. If you are waiting to use SystemVerilog until a year from now, you are falling behind! Now is the time to learn and adopt SystemVerilog methodologies, capabilities and techniques.”

-- *Clifford E. Cummings, President, Sunburst Design, Inc.*

Sutherland HDL, Inc.

“The formal approval of the IEEE 1800 SystemVerilog marks a significant milestone for users of the Verilog language. Just as significant is how rapidly proactive EDA companies have implemented these important extensions to the Verilog language. At Sutherland HDL, we have seen a marked upsurge in requests for our advanced SystemVerilog training workshops, an indication that design and verification engineers are ready and anxious to benefit from SystemVerilog in current and upcoming IC design projects.”

-- *Stuart Sutherland, Principle Engineer, Sutherland HDL, Inc.*

SynaptiCAD

“SynaptiCAD is currently enhancing our test bench generation software, TestBencher Pro, to support SystemVerilog verification environments and to generate test benches from graphical timing diagrams. Features such as the SystemVerilog interface construct really add to the re-usability and maintainability of system level test benches.”

-- *Dan Notestein, President, SynaptiCAD*

Verific Design Automation

“At Verific Design Automation we are very happy with the IEEE 1800 standard. As the premier provider of SystemVerilog front-ends to the EDA, we at times felt we were chasing a constantly evolving language. Now we and our customers can concentrate on a

single standard that will bring much needed stability to the field. EDA users will soon see a variety of EDA tools being brought on the market based on Verific's 1800 front-end.”

-- Michiel Ligthart, Chief Operating Officer, Verific Design Automation

Verilab

“Verilab welcomes the ratification of the IEEE 1800 SystemVerilog standard. By providing specific functional coverage, constrained-random, and object-oriented features, SystemVerilog enhances our clients' abilities to develop highly reusable coverage-driven verification environments, capable of handling very complex designs. SystemVerilog Assertions provide a concise and effective way for design and verification teams to describe and check behavior and a convenient gateway to static formal verification. We believe these features provide a significant and essential step up from traditional HDLs in managing the complexity of today's designs. Verilab will continue to develop SystemVerilog methodology and services to help our clients implement solutions effectively on their projects.”

-- Jason Sprott, VP Consulting, Verilab

VhdlCohen Publishing

“Current training based on our "SystemVerilog Assertions Handbook" is proving very beneficial for designers' verification methodologies. Our next book will use a simple, but complete example, to illustrate the application of VMM for SystemVerilog validation strategies.”

-- Ben Cohen, VhdlCohen Publishing

XtremeEDA

“As verification professionals we have long felt that the industry required a verification technology clearly separated from any single vendor. IEEE standard 1800 combines the robustness of legacy Verilog technology with the latest advances in verification methodology to deliver an open standard upon which more complex designs can be based. XtremeEDA is pleased to integrate the committee's hard work into its first-class training and methodology development consulting services. Now that the standard has been approved, we expect rapid industry adoption driven by its implementation by multiple vendors.”

-- Michael Faltas, Vice President of Sales, XtremeEDA

Yogitech

“We welcome the achievement from IEEE and Accellera; as a verification IP provider, we look at interoperability as a key factor to further enable the success of our VIPs on the market. IEEE 1800™-2005 is a crucial milestone in that direction and we can now plan an extension to SystemVerilog for our VIPs' portfolio currently including solutions for OCP, CAN, LIN, Parallel ATA and the recently announced Mixed Signal Verification Kit.”

-- Silvano Motto, CEO of Yogitech