

Advisory

**Accellera Co-Sponsors and Supports SystemVerilog and PSL Electronic Design Automation
Standard Sessions at the FORUM on Specification & Design Languages**

September 27-30, 2005, Lausanne, Switzerland

Who

Accellera, the Electronic Design Automation (EDA) organization focused on language-based design standards, invites the electronic design community to attend sessions at the FORUM on Specification & Design Languages (FDL '05) in Lausanne, Switzerland, an event co-sponsored by the organization.

What

Members of Accellera's groups will present an overview of the SystemVerilog Hardware Design and Verification Language standard (HDVL), also known as IEEE P1800, and a session on the Property Specification Language (PSL) standard, also known as IEEE Std™ 1850.

When

SystemVerilog in Action

900-1300, Wednesday, 28 September

PSL Session

11:30-15:50, Friday, 30 September

Where

Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland.

For More Information

For more information about FDL '05, please visit <http://www.ecsi-association.org/ecsi/fdl/fdl05/>.

For more information about Accellera and Accellera standards, please visit www.accellera.org.

About PSL

The PSL standard addresses the shortcomings of natural language forms of design specification. It allows engineers to capture the functional specifications of logic design in a way that is unambiguous, effective and concise using the notion of properties and assertions. The expressiveness of PSL allows users to easily document and specify design behavior with properties. Furthermore, the formal nature of PSL enables the use of automatic tools to verify design properties written in this language, saving time and effort in the design verification cycle.

About SystemVerilog

SystemVerilog is a unified hardware design, specification and verification language standard that is based on the work done by Accellera. It adds powerful design and verification capabilities to the Verilog hardware description language (HDL) with constructs for architectural, algorithmic and transaction-based modeling. It

also offers an environment for automated testbench generation, and provides assertions to describe design functionality, including complex protocols, to drive verification using simulation or formal verification techniques. Its C-API (Application Programming Interface) provides the ability to mix Verilog HDL and C/C++ constructs.

About Accellera

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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