

Accellera Co-Sponsors 3rd SystemVerilog Design Workshop in Japan

Friday, November 11, 2005

Who

Accellera, the Electronic Design Automation (EDA) organization focused on language-based design standards, is a sponsor of CQ Publishing's 3rd SystemVerilog Design Workshop. At the event, Accellera's vice-chairman, Dennis Brophy will speak about Accellera's SystemVerilog unified Hardware Design, Specification and Verification Language standard also known as IEEE Std.1800™-2005.

When/What/Where:

Date: Friday, November, 11, 2005

Time: 15:00 – 16:00

Presentation: *IEEE Std. 1800™-2005: The Making and Celebration of the World's First Hardware Design Specification and Verification Language (HDVL)*

Location: 3rd Floor, Room 2, TEPIA, 2-8-44 Kita Aoyama, Minato-ku, Tokyo, Japan

<http://www.tepia.jp/english/index.html>

Time: 16:30

Reception: Happy Birthday Celebration for IEEE Std. 1800-2005

Location: 2nd Floor, TEPIA

The reception is hosted by Accellera, and supported by Synopsys and Mentor Graphics

For More Information:

For more information about Accellera and Accellera standards, please visit www.accellera.org.

For more information about the CQ event, please visit <https://it.cqpub.co.jp/tse/DW200511/>.

About SystemVerilog

SystemVerilog expands language-based electronic design with new and powerful design and verification capabilities, fully aligned with and built upon the Verilog-2005 standard, IEEE Std.1364™-2005. Its enhancements include the extension of memory system tasks for complex memory modeling, operator overloading for simplified expressions, and tagged unions with pattern matching for code conciseness and improved formal analysis. Assertion enhancements span environmental constraints to facilitate formal analysis and random simulation, and a broader scope of assertions for more comprehensive behavior and design intent specification. Testbench generation improvements encompass fine-grain process control for multi-threaded testbench development;

dynamic and static queues with stream generation for complex verification scenarios; virtual interfaces for expressiveness of testbench infrastructure; and random weighted case plus functional coverage.

About Accellera

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera's partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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