

For Immediate Release

Accellera Approves New Open Verification Library Standard

First Native SystemVerilog Assertion Version & Improved Verilog Library of Checkers Available

NAPA, California—August 24, 2005 Accellera, the electronics industry organization focused on electronic design automation (EDA) standards, today announced that its Board of Directors, representing systems, semiconductor and design tool member companies, approved Accellera's **Open Verification Library (OVL) 1.0**, as an Accellera verification standard earlier this month. The new standard was also approved unanimously by the Accellera OVL Verilog/SystemVerilog Assertion (OVL-VSVA) technical committee.

The OVL standard results in better quality HDL (hardware description language) designs, since the pre-defined checkers, written in either Verilog or SystemVerilog, allow designers to take advantage of assertion-based verification immediately. Both SystemVerilog and Verilog language-compliant tools can take advantage of this new verification standard. The library includes 31 assertion checkers for each language that cover many of the common properties that engineers check during the functional verification of register-transfer level (RTL) code.

“Our OVL standard allows for better and higher quality standards-based solutions that improve verification and verification productivity for electronic design teams,” said Dennis Brophy, Accellera chairman. “The global electronic industry is in debt to the dedication and commitment of the OVL committee for delivering this important contribution in record time.”

“Our committee was able to work through the standardization process in 4 months to address critical verification challenges,” said Kenneth Larsen, Accellera OVL-VSVA technical committee chair. “By using a single well-defined interface, OVL bridges the gaps among different types of verification processes, making more advanced verification tools and techniques available for non-expert users.”

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More about the OVL Standard

The OVL standard for Verilog and SystemVerilog assertions addresses the needs of designers, integrators and verification engineers to check for expected and unexpected behavior with a single vendor-independent interface for design validation using simulation, semiformal and formal verification techniques.

Accellera OVL assertion checkers allow designers and verification engineers to instrument their designs to detect design failures closer to their origin for faster error detection discovery and resolution.

This is the first release of the Accellera standard to leverage the SystemVerilog assertion syntax using IEEE P1800 “SystemVerilog.” The Accellera standard also supports assertions written in IEEE Std™ 1364-1995 “Verilog” to ensure the entire Verilog community can immediately use this new standard.

The work of the OVL-VSVA committee includes a Library Reference Manual and assertion checkers written for Verilog and SystemVerilog that cover many common properties that engineers use during assertion-based and coverage-driven verification.

OVL Availability

The Accellera Standard Open Verification Library v1.0 for Verilog and SystemVerilog is available now for download at the Accellera website: www.accellera.org.

About Accellera

Accellera provides design standards for quick availability and use in the electronics industry. The organization and its members cooperatively deliver much-needed EDA standards that lower the cost of designing commercial IC and EDA products. As a result of Accellera’s partnership with the IEEE, Accellera standards are provided to the IEEE standards body for formalization and ongoing change control. For more information about Accellera, please visit www.accellera.org.

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