Cliff's vote - email vote submitted on 20060202:

Yes on: 871, 881, 908, 912, 932, 941, 942, 944, 945, 952, 961, 984, 1092, 1138, 1159, 1253, 1260, 1261, 1297 (close as already fixed?), 1298

No on: 882, 911, 919, 946, 949, 962, 1255.
(see below)

No on SVDB 882
Reason - make the example useful. Show a list of arrayed real declarations (not shown elsewhere).
WAS:
var real `y, z;`

PROPOSED:
var real `y [0:1] = '{0.0, 1.1}, z [0:9] = '{default: 3.1416};`

No on SVDB 911
Reason - new wording is still improper English.
WAS:
The C **`float`** type is called **`shortreal`** in SystemVerilog ~~so that it is not be confused~~ with the Verilog **`real`** type.

PROPOSED:
The C **`float`** type is called **`shortreal`** in SystemVerilog to avoid confusion with the Verilog **`real`** type.

No on SVDB 919
No particular objection, but there has been a large number of email messages regarding $bits so I would just like to hear everyone express no objection on a conference call. If this is as easy as claimed, I believe this can be approved quickly on our next conference call.

No on SVDB 946 - Friendly amendment
While we are fixing the formatting, let's also create a 2-line comment since the existing comment spills onto the next line, which could be confusing:
WAS:
```
~~reg~~ [7:0] r1 [1:256]; // [7:0] is the vector width, ~~[1:256] is the array size~~
```

PROPOSED:
```
reg [7:0] r1 [1:256]; //   [7:0] is the vector width,
                      // [1:256] is the array size
```

No on SVDB 949
Shalom's proposed fix is fine, but it may be a more instructive example if we make the small fix to allow 32-bit unsigned bit-type variables to be assigned to the signed integers and enhance the final comment as shown:
WAS:

```
bit busA [7:0] [31:0] ; // unpacked array of 8 32-bit vectors
int busB [1:0];         // unpacked array of 2 integers
busB = busA[7:6];       // select a slice from busA
```

PROPOSED:

```
bit [31:0] busA [7:0]; // unpacked array of 8 32-bit vectors
int        busB [1:0]; // unpacked array of 2 integers
busB = busA[7:6];      // select a 2-vector slice from busA
```

No on SVDB 962 - I could not find the referenced error in the 1364-D7 document.

No on SVDB 1255 - I could go either way on this but I believe Shalom is correct that at least UDP "ports" are really terminals (described as ports in at least 1364-2005-D7, clause 8.1.1), in that they can only be 1-bit in width and when instantiated, UDP's cannot be instantiated using named "ports" (they behave just like a real primitive).