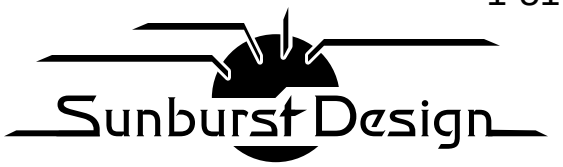
Configuration Limitation
(Verilog-1995 Limitation)



- One Verilog configuration limitation
  - Mixing gate and behavioral instances in the same design
  - Example: 3 RTL Adders, 1 gate-level Adder

- The Cadence approach (not in IEEE-1364 Standard)
  - `uselib compiler directive (supported by VCS & ModelSim):

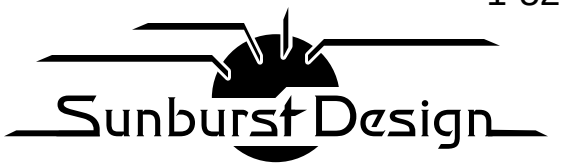
```
`uselib dir=/proj/design/vlog libext=.v
Adder i1 (…);                    // from vlog directory
Adder i3 (…);                    // from vlog directory
Adder i4 (…);                    // from vlog directory
`uselib dir=/proj/design/gates libext=.v
Adder i2 (…);                    // from gates directory
`uselib
```

UGLY!!
Requires modification to the source code to run different simulations

Not synthesizable

Verilog Configuration Keyword

Verilog-2001 Enhancement #5



- Verilog configuration file keywords

```
config
  ...
endconfig
```

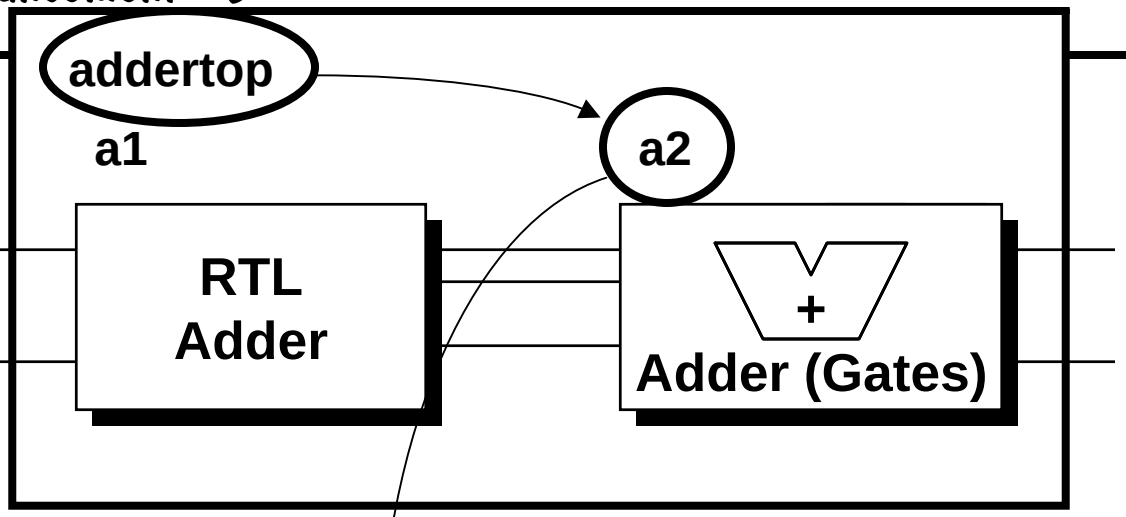
- VHDL configuration file keywords

```
configuration
  ...
end configuration
```

- EDA vendors wanted an easy way to distinguish between Verilog & VHDL:
  - to enable *co-compiled designs*
  - to enable *co-simulated designs*

Verilog Configuration Files

Verilog-2001 Enhancement #5



Simulation specification #1
addertop.a1 - RTL model
addertop.a2 - RTL model

file: `rtl.cfg`

```
config rtl;
  design   rtlLib.addertop;
  default  liblist rtlLib;
endconfig
```

Simulation specification #2
addertop.a1 - RTL model
addertop.a2 - gate-level model

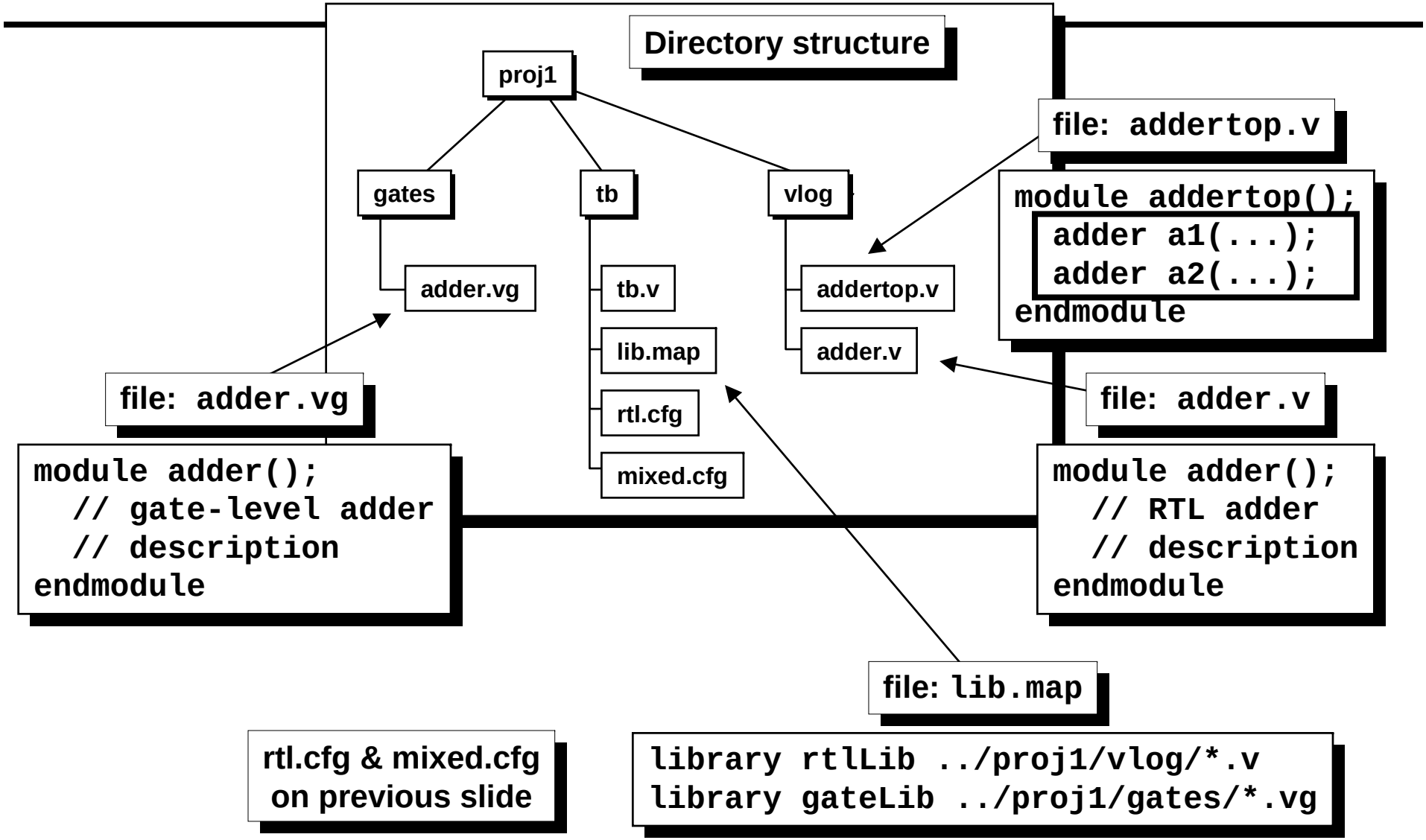
file: `mixed.cfg`

```
config mixed;
  design   rtlLib.addertop;
  default  liblist rtlLib;
  instance addertop.a2 liblist gateLib;
endconfig
```

Libraries on the next slide

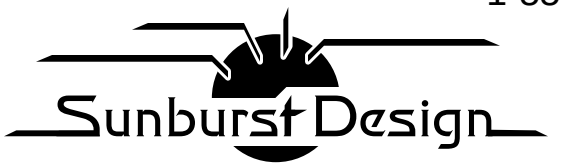
Different Simulation Configurations

Verilog-2001 Enhancement #5



Different Simulation Configurations

Verilog-2001 Enhancement #5



RTL simulation

Verilog-1995 Command line switches

```
verilog tb.v -y ../vlog +libext+.v
```

Gates simulation

```
verilog tb.v -y ../gates +libext+.vg
```

file: lib.map

```
library tbLib   ../proj1/tb/*.v;
library rtlLib  ../proj1/vlog/*.v;
library gateLib ../proj1/gates/*.vg;
```

file: rtl.cfg

```
config rtl;
  design   tbLib.tb;
  default  liblist rtlLib;
endconfig
```

file: gates.cfg

```
config gates;
  design   tbLib.tb;
  default  liblist gateLib;
endconfig
```

file: mixed.cfg

```
config mixed;
  design   tbLib.tb;
  default  liblist rtlLib;
  instance addertop.a2 liblist gateLib;
endconfig
```

Not easy with Verilog-1995 without ugly `uselib directives