## Proposal to fix keyword compatibility issues between 1364 and P1800

Add new section 25.4, as follows:

## 25.4 keywords, endkeywords

SystemVerilog provides a pair of directives, 'keywords and 'endkeywords, that specify what identifiers are reserved as keywords within a block of source code, based on a specific version of the IEEE 1364 Verilog standard or the IEEE 1800 SystemVerilog standard.

The 'keywords and 'endkeywords directives only specify the set of identifiers that are reserved as keywords. The directives do not affect the semantics, tokens and other aspects of the Verilog and SystemVerilog languages.

The syntax of the 'keywords and 'endkeywords directives are:

```
keywords_directive ::= `keywords version_specifier
version_specifier ::=
   "default"
   | "1364-1995"
   | "1364-2001"
   | "1364-2005"
   | "1364-latest"
   | "1800-2005"
   | "1800-latest"
endkeywords_directive ::= `endkeywords
```

The 'keywords directive can only be specified outside of a module, primitive, interface, program or package. It affects all modules, primitives, interfaces, programs or packages that follow the directive, even across source code file boundaries. Multiple 'keywords directives are allowed. The latest occurrence of the directive in the source code controls the set of identifiers that are reserved keywords for the source code that follows the directive.

If no 'keywords directive is specified, then the default reserved keyword list shall be implementation dependent. The lack of a 'keywords directive is the same as if the directive 'keywords "default" had been specified.

The directives 'endkeywords and 'resetall shall terminate the effect of the 'keywords directive. 'endkeywords and 'resetall have the same effect as 'keywords "default".

The <code>version\_specifier</code> "default" specifies that the implementation determines the set of reserved keywords that are in effect. For example, an implementation based on the IEEE 1364-2005 Verilog standard would most likely use the 1364-2005 set of reserved keywords as its default. Another possible use model might be that an implementation provides invocation options to establish the legal set of default keywords.

The *version\_specifier* "1364-1995" specifies that only the identifiers listed as reserved keywords in the IEEE 1364-1995 standard are considered to be reserved words. These identifiers are listed in Table 25-1.

Table 25-1: IEEE 1364-1995 reserved keywords

always	for	pmos	supply1
and	force	posedge	table
assign	forever	primitive	task
begin	fork	pull0	time
buf	function	pull1	tran
bufif0	highz0	pullup	tranif0
bufif1	highz1	pulldown	tranif1
case	if	rcmos	tri
casex	initial	real	tri0
casez	inout	realtime	tri1
cmos	input	req	triand
deassign	integer	release	trior
default	9		
	join	repeat	trireg
defparam	large	rnmos	unsigned
disable	macromodule	rpmos	vectored
edge	medium	rtran	wait
else	module	rtranif0	wand
end	nand	rtranif1	weak0
endattribute	negedge	scalared	weak1
endcase	nmos	signed	while
endmodule	nor	small	wire
endfunction	not	specify	wor
endprimitive	notif0	specparam	xnor
endspecify	notif1	strength	xor
endtable	or	strong0	
endtask	output	strong1	
event	parameter	supply0	

The *version\_specifier* "1364-2001" specifies that only the identifiers listed as reserved keywords in the IEEE 1364-2001 standard are considered to be reserved words. These identifiers are listed in Table 25-2.

The *version\_specifier* "1364-2005" specifies that only the identifiers listed as reserved keywords in the IEEE 1364-2005 standard are considered to be reserved words. These identifiers are listed in Table 25-2.

Table 25-2: IEEE 1364-2001 and 1364-2005 reserved keywords

_			
always	event	noshowcancelled	specify
and	for	not	specparam
assign	force	notif0	strong0
automatic	forever	notif1	strong1
begin	fork	or	supply0
buf	function	output	supply1
bufif0	generate	parameter	table
bufif1	genvar	pmos	task
case	highz0	posedge	time
casex	highz1	primitive	tran
casez	if	pull0	tranif0
cell	ifnone	pull1	tranif1
cmos	incdir	pulldown	tri
config	include	pullup	tri0
deassign	initial	pulsestyle_onevent	tri1
default	inout	pulsestyle_ondetect	triand
defparam	input	rcmos	trior
design	instance	real	trireg
disable	integer	realtime	unsigned
edge	join	reg	use
else	large	release	vectored
end	liblist	repeat	wait
endcase	library	rnmos	wand
endconfig	localparam	rpmos	weak0
endfunction	macromodule	rtran	weak1
endgenerate	medium	rtranif0	while
endmodule	module	rtranif1	wire
endprimitive	nand	scalared	wor
endspecify	negedge	showcancelled	xnor
endtable	nmos	signed	xor
endtask	nor	small	-

The *version\_specifier* "1800-2005" specifies that only the identifiers listed as reserved keywords in the IEEE 1800-2005 standard are considered to be reserved words. These identifiers are listed in Table 25-3.

Table 25-3: IEEE 1800-2005 reserved keywords

alias	endinterface	longint	shortreal
always	endmodule	macromodule	showcancelled
_	endpackage	matches	signed
always_comb		medium	small
always_ff	endprimitive		
always_latch	endprogram	modport module	solve
and	endproperty		specify
assert	endspecify	nand	specparam
assign	endsequence	negedge	static
assume .	endtable	new	string
automatic	endtask	nmos	strong0
before	enum	nor	strong1
begin	event	noshowcancelled	struct
bind	expect	not	super
bins	export	notif0	supply0
binsof	extends	notif1	supply1
bit	extern	null	table
break	final	or	tagged
buf	first_match	output	task
bufif0	for	package	this
bufif1	force	packed	throughout
byte	foreach	parameter	time
case	forever	pmos	timeprecision
casex	fork	posedge	timeunit
casez	forkjoin	primitive	tran
cell	function	priority	tranif0
chandle	generate	program	tranif1
class	genvar	property	tri
clocking	highz0	protected	tri0
cmos	highz1	pull0	tri1
config	if	pull1	triand
const	iff	pulldown	trior
constraint	ifnone	pullup	trireg
context	ignore_bins	pulsestyle_onevent	type
continue	illegal_bins	pulsestyle_ondetect	typedef
cover	import	pure	union
covergroup	incdir	rand	unique
coverpoint	include	randc	unsigned
cross	initial	randcase	use
deassign	inout	randsequence	var
default	input	rcmos	vectored
defparam	inside	real	virtual
design	instance	realtime	void
disable	int	ref	wait
dist	integer	reg	wait_order
do	interface	release	wand
edge	intersect	repeat	weak0
else	join	return	weak1
end	join_any	rnmos	while
endcase	join_none	rpmos	wildcard
endclass	large	rtran	wire
endclocking	liblist	rtranif0	with
endconfig	library	rtranif1	within
endfunction	local	scalared	WOT
endgenerate	localparam	sequence	xnor
endgroup	logic	shortint	xor
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The version\_specifier "1364-latest" specifies that only the identifiers listed as reserved keywords in the most current official version of IEEE 1364 standard are considered to be reserved words.

The version\_specifier "1800-latest" specifies that only the identifiers listed as reserved keywords in the most current official version of IEEE 1800 standard are considered to be reserved words.

In the example below, it is assumed that the definition of module m1 does not have a 'keywords directive specified prior to module definition. Without this directive, the set of reserved keywords in effect for this module shall be the implementation's default set of reserved keywords

```
module m1; // module definition with no `keywords directive
   ...
endmodule
```

The following example specifies a 'keywords directive on an **interface** declaration. The directive specifies that an implementation shall use the set of reserved keywords specified in the IEEE 1800-2005 SystemVerilog standard.

The next example is nearly identical to the one above, except that the 'keywords directive specifies that the IEEE 1364-2005 Verilog set of keywords shall be used. This example shall result in errors, because the identifiers "interface" and "interface" are not reserved keywords in the IEEE 1364-2005 Verilog standard.