Section 18.3 (New)

Add (change in red):

18.3 Compilation Unit Support

SystemVerilog supports separate compilation using compiled units. The following terms and definitions are provided:

— compilation unit: a collection of one or more SystemVerilog source files compiled together
— compilation-unit scope: a scope that is local to the compilation unit. It contains all declarations that lie outside of any other scope
— $unit: the name used to explicitly access the identifiers in the compilation-unit scope

The exact mechanism for defining which files constitute a compilation unit is tool specific. Tools shall provide a mechanism to specify the files that make up a compilation unit. Two extreme cases are:

1. All files make a single compilation unit (in which case the declarations in the compilation-unit scope are accessible anywhere within the design)
2. Each file is a separate compilation unit (in which case the declarations in each compilation-unit scope are accessible only within its corresponding file)

The contents of files included using one or more ‘include directives become part of the compilation unit of the file they are included within.

If there is a declaration that is incomplete at the end of a file then the compilation unit including that file will extend through each successive file until there are no incomplete declarations at the end of the group of files.

The default is that each file is a separate compilation unit.

A tool must also provide a mechanism (such as a command line switch) that specifies that all of the files compiled together are a single compilation unit.

There are other possible mappings of files to compilation units and the mechanism for defining them are tool specific and may not be portable.