SV-DC Scope:

The SV-DC committee will investigate and recommend a roadmap for discrete modeling features within SystemVerilog. Limiting the scope to discrete modeling means there is not an intention to bring the analog solver into SystemVerilog. The near term roadmap will likely include nets and ports of generic data types, resolution functions, and type conversion mechanisms. Longer term, the roadmap may include features for piece-wise linear waveform definition and support for several modeling styles (e.g., timed data driven, signal flow, modeling with restricted conservative linear networks). It is expected that these features can exist in SystemVerilog without requiring a merge of the SystemVerilog and Verilog-AMS standards.

The primary use case motivating this work is the need for high speed simulation of models of analog blocks. Faster discrete models will be interchangeable in a plug and play style with continuous or conservative models.

The roadmap will focus on the items to be completed within the 2012 PAR, but will also provide vision for future directions. It will identify the new discrete modeling features and describe how they will interact with current SystemVerilog features. It may also include recommendations of how these features interact with VHDL and/or Verilog-AMS. The initial roadmap will be completed no later than September 15, 2010.

0. Executive Summary

SV-DC intends to provide capabilities in SystemVerilog to support efficient modeling of analog/mixed-signal circuit components. These models are to be simulated by the event-driven simulation engine and should, therefore, exhibit simulation performance comparable to digital models and be suitable for system level simulation. The new modeling capabilities will be achieved by natural extensions to the existing SystemVerilog language; no analog solvers or netlist manipulations will be required.

1. Motivation and Use Cases [why]

The primary use case motivating SV-DC's work is the need for high speed simulation of models of analog blocks. Existing analog/mixed-signal simulations are not sufficiently scalable to accommodate platform and system level models. The envisioned solution is to enable modeling of such blocks in the discrete domain, trading accuracy for speed. Faster discrete models will be interchangeable in a plug and play style with continuous or conservative models.

Effective discrete domain real-valued modeling will require natural extensions to SystemVerilog, such as real-valued nets and ports, aggregate nets and ports involving real values, resolution functions, generic interconnects, and type conversion mechanisms. These modeling capabilities will support uses such as:

-Design exploration and verification of large mixed-signal systems.

-Representing the inter-connect of an entire system.

-Modeling mixed use signals. For example, the same wire may be driven at some times by a digital clock and at other times by an analog voltage.

-Easy swapping of models with differing levels of abstraction but compatible interfaces.

2. Requirements [what]

Note: Each requirement has a priority assigned to it. These priorities are contained in brackets. The priorities are MUST, SHOULD, and COULD. Items at the MUST priority level are required for a complete user solution. SV-DC intends to complete these items in this PAR. If they are not completed an explanation of the primary difficulties in devising a solution will be provided. Items at the SHOULD priority level are items that provide high value to the user community. Items at the COULD level are lower priority and can be handled if time permits or an easy solution arises.

A. Net Capabilities

Scalar Real Valued Net

R01. [MUST] Real valued nets with multiple drivers

R02. [MUST] Resolution functions for multiply driven real valued nets

R03. [MUST] Ability to represent X (unknown) and Z (undriven/high impedance) states for real nets

R04. [MUST] Unidirectional and bidirectional ports with real nets

Aggregate Nets with Real Valued Components

R05. [MUST] Aggregate nets with real valued components, including constructs such as vectors, static arrays, structs, unions

R06. [MUST] Resolution functions for multiply driven aggregate nets

R07. [MUST] Unidirectional and bidirectional ports with aggregate nets

R08. [MUST] Atomic aggregate nets whose components are resolved jointly (correlated resolution)

R09. [MUST] Ability to represent X (unknown) and Z (undriven/high impedance) states for atomic aggregate nets

R10. [SHOULD] Discuss ways of modeling state and scheduling events in aggregate nets

B. Type Conversion and Compatibility

R11. [SHOULD] Type conversion mechanisms to enable connection of nets of different, yet compatible, types and structures, including connection of aggregate nets

R12. [SHOULD] Ensure design intent is clear when converting from logic to real valued domains, including voltage intent for signals

R13: [SHOULD] Mechanisms for type conversions to access nominal and actual power supplies (for accurate conversion of logic values to voltages etc.).

C. Utilities for Real Modeling

R14. [SHOULD] Generic interconnect constructs for structural connectivity

R15. [SHOULD] Type coercion between generic interconnect and explicit types

R16. [SHOULD] Capability to create aggregates of generic interconnect where individual selects or slices may connect to ports of different types

R17. [MUST] Definitions of math functions and relational operators for real types in the presence of unknown and high impedance states

R18. [COULD] VCD support for newly introduced nets

R19. [COULD] VPI support for newly introduced nets including force/release/deposit and similar operations

R20. [COULD] Delay on newly introduced nets

R21: [COULD] Mechanisms for back-annotating circuitry (parasitics and wiring) that work with the above mechanisms (so that post place-and-route simulations will work with the models using user-defined wire types).

D. Items for future PARs

R22. [COULD] Enhanced real-valued net state with quasi-continuous signal functions, time constants, next-time points for reevaluation, etc.

R23. [COULD] $tablemodel support with real net type

R24. [COULD] Specification of dense time characteristics (e.g., slewed delay transition of a net, piecewise linear representation of the value of a net)

R25. [COULD] Ability to model power supply/domain on a real value net

3. Relationship to Verilog-AMS

Verilog-AMS is part of the Verilog family of languages and has been standardized By Accellera. It is the Accellera plan that Verilog-AMS merges with SystemVerilog at some point in the future so that there is unified standard covering all the Verilog languages.

SV-DC is aware that the proposed discrete domain real modeling capabilities will have some level of overlap with the capabilities provided by Verilog-AMS wreal. SV-DC is also aware that work to merge SystemVerilog and Verilog-AMS has started and a draft document is due for completion at the end of 2011. At that point, the draft is intended to be donated to IEEE for inclusion in the SV standardization process. SV-DC itself intends neither to merge wreal into SystemVerilog nor to complicate this merger. Therefore SV-DC will study the mapping of Verilog-AMS wreal capabilities into the new real modeling framework. The expectation of SV-DC is that the overlapping functionality of Verilog-AMS wreal will map reasonably into the new SystemVerilog real modeling framework. SV-DC will communicate the results of this study to the Verilog-AMS Committee as an aid to merger activities. SV-DC will also take account of this study and feedback on it before finalizing 2A.

Subgroups of the Verilog-AMS and SV-DC committees will meet regularly to discuss technical issues of interest between the two committees.

4. Timeline and Vision [when]

SV-DC intends to address requirements marked with MUST and SHOULD priority in the timeframe of the 2012 Standard Requirements marked with COULD priority will be addressed in the 2012 Standard as time permits or in future PARs.