Mantis 2889

.named_port(expression) in ANSI-style port declaration list should reset properties

In Section 23.2.2.3

ADD at the end of the section:

The preceding rules do not apply to explicit port declarations (i.e., of the form *.port_identifier(expression)*, see 23.2.2.2). Explicit port declarations shall inherit only the port direction from the preceding port (if not explicitly specified), but not other properties. The data type of the port is the self-determined data type of the *expression*.

A port declaration that immediately follows an explicit port declaration shall inherit only the port direction (if not explicitly specified) from the explicit port declaration, but not other properties. The port kind and data type of such a port shall be determined using the same rules as for the first port in the port list.

Example:

```
module mh22 (input wire integer p_a, .p_b(s_b), p_c);
logic [5:0] s_b;
```

In this example, port `p_a` is fully declared. `p_b` is an explicitly named port that inherits only the direction **`input`** from port `p_a`. Its data type is that of `s_b`. Port `p_c` inherits only the direction from `p_b`, and defaults to the net port kind and to the **`logic`** data type.