Mantis 2889

.named_port(expression) in ANSI-style port declaration list should reset properties

In Section 23.2.2.3

ADD at the end of the section:

The preceding rules do not apply to explicitly named port declarations (see 23.2.2.2). Explicitly named ports inherit only the port direction from the preceding port, but not other properties. The port kind and data type are determined by the port expression. Subsequent port declarations may inherit only the port direction from the explicitly named port declaration, but not other properties. The port kind and data type of a port declaration that immediately follows an explicitly named port declaration shall be determined using the same rules as for the first port in the port list.

Example:

```
module mh22 (input wire integer a, .B(b), c); // input wire integer a
logic [5:0] b;                                //(input)var logic[5:0] b
                                              // input wire logic c
```

In this example, port a is fully declared. Port B is an explicitly named port that inherits only the direction **`input`** from port a. Port c inherits only the direction from port B, and defaults to the net port kind and to the **`logic`** data type.