LRM-1

The following sections can change parameter to argument
1 4.6.1 4.8 10.5.2 10.5.4 12.6

The following section should remain as they are (use of parameter is appropriate here)
13.3.5 13.4 15.3

Section **13.8** was to be removed and the example folded into the event control section.

In section **15.2** "parameters determine" can be changed to "specifications determines".

LRM-2

In section **18.7** the use of parameters is appropriate and no change is needed.

LRM-3

In section **2.5** "actual parameter" refers to the Verilog parameter specified in the module instance.

LRM-7

In section **3.8.9** the use of integer is correct. This is because the string can include 'X' or 'Z'.

LRM-8

In section **3.10** the use of "may not" should be changed to "is not allowed to" or "shall not"

LRM-10

In section **8.10** , ->> is not an operator (just like ->) and dies not need to be in the operator table.
It's use is completely defined via BNF (need BNF for this).

LRM-14

The precedence of the :: operator described in section **11.20** should be the same as . (highest).

LRM-16

The precedence of the **inside** operator described in section **12.4.3** is already defined in the table.

LRM-17

The precedence of the **dist** operator described in section **12.4.4** is already defined in the table.

LRM-18

The := and :/ operators (in section **12.4.4**) have the precedence of assignment. They do not strictly need it since they are top-level operators so the grammar (BNF) is sufficient.
LRM-19

The precedence of the => operator described in section **12.4.5** is already defined in the table.

LRM-20

A constraint is not a data-type, thus, the use of 'static constraint' in section **12.4.9** is consistent.

LRM-21

In section **12.10.1** "unsigned int" should be changed to "int unsigned"

LRM-22

In section **12.10.2** "unsigned int" should be changed to "int unsigned"

LRM-23

In section **12.10.3** "object obj" should be changed to "object_identifier"