SystemVerilog Committee Meeting (Let Us Roll)

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Agenda

- 9:00 - 9:15 Introduction Vassilios Gerousis
- 9:15 - 10:15 SV committee status (all four committees).
  - SV Basic Johny Srouji / Karen Pieper
  - SV Assertion Faisal Haque/Stephen Meier
  - SV C interface Swapnajit Mittra/Ghassan Khoory
  - SV Enhancement David Smith/Stefen Boyd
- 10:15 - 10:30 Break
- 10:30 - 12:00 Synchronization, scheduling, SV 4.0
- 12:00 - 12:30 Lunch
- 12:30 - 2:30 Technical Presentation (Technical Content)
  - Unified Assertion (SVA): Latest SVA LRM. (0.5 hour)
  - SVC (Direct-C, etc): Latest SVC LRM (0.5 hour)
  - Changes expected or proposed by basic (0.5 hour).
  - Testbench (SVT): Latest LRM and completed proposals.
- 2:30 - 2:45 Break
- 2:45 - 3:00 Patent Discussions ALL
- 3:00 - 4:00 Completion Plans For SV 3.1 SV Chairs
- 4:00 - 4:30 Summary and Actions.

SV committees accomplishment

- All four committee are meeting the SV Chairs Milestone:
  - Draft 3 of SV 3.1 for
    - SVT (SystemVerilog Testbench).
    - SVA (SystemVerilog Assertions).
    - SVC (SystemVerilog C/API Interface) - DPI is also on the table.
    - SVD (SystemVerilog Design (Core Technology)).
- My deepest thanks to the SV Chairs for leadership and for all participants!
- Accomplished two major architectural design:
  - David Smith lead SSWG and finalized Simulation semantics.
  - Karen Pieper lead $root committee and proposed changes.

Verisity Patent (6,141,630)

- Michael McNamara Sent an email to SV-CC committee and declared Patent 6,141,630.
- Expert Analysis (Not a lawyer, Nor Accellera)
  - (claim 2, 3) a notion of transitions and transition coverage.
  - (claim 4) is limited to synthesizable designs
  - (claim 5) an automated test vector generator driven from a model created by analysis of the design.
- As far as I am aware, neither the coverage technologies donated to SV-CC by Synopsys
- Nor the coverage proposals agreed to by SV-CC infringe on the above claims.
- SystemVerilog is just a language, not a particular simulator implementation.
- Both **Users** and **Vendors** could violate the patents claims by using VHDL, SystemC or SystemVerilog.

Patents

- Verisity Patent Is Irrelevant in regards to SystemVerilog as a standard language.
- I have asked Verisity through the Accellera Board to explain their motivation.
  - Three months has passed and no feedback.
- In December, I also challenged 0-IN to provide explanation of their intentions.
  - Again they have refused to do so.
- Any Additional Comments is welcomed.

LRM Completion Schedule

- February 2003: Stable LRM - Language design is complete.
- March 2003
  - 1st week freeze issues;
  - 2nd week all resolved;
  - 3rd week complete draft;
    - (**Draft 4** need version with change bars and without)
- April 2003
  - 1st of April send document to Accellera member companies;
  - End of April document freeze date and voted on by each committee
    - (for their own work) (**Draft 5**)
- May2003
  - 1st week send to TCC and to board
  - End of May vote is complete
- June 2 - SystemVerilog 3.1 Standard LRM Published.

Committee Independent Check

- 3 to 6 experts in the industry will be reviewing the LRM:
  - There are not part of any committee within Accellera.
  - A request to participate will be sent today.
  - Invitation only.
  - Provide feedback for clarification.
- BNF creation:
  - Stephen Boyd will generate a complete Verilog+SystemVerilog BNF.
  - Dan Jacobi of Intel will help from SV-BC.
  - Others will be called as needed.

HDL+ Committees