# SV-AC status
# Feb 03


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# Assertion Requirements Met by SVA

- SystemVerilog integrated assertion language
  - Uses Verilog for Boolean and bit vector expressions
  - Designed for ease of use with regular expressions, intuitive syntax
  - Features defined for testbench, coverage,  and formal verification
- Common cycle based semantics for both simulation and formal
- Unified assertion support for all SystemVerilog applications (RTL, testbench, coverage, formal)
  - Support both declarative and embedded procedural asserts
  - Template/library features for assertion libraries and re-use

# SVA Changes from DAS 1.0

Improved concurrent assertions

- Sampling – cycle based semantic (formal, H/W accelerator)
- Embedding in procedural code

Expanded expressive power

- Sequence operations (and, or, intersect)
- Property declaration and instantiation
- Property formulas and directives

Restricted immediate assertions (check)

- Limit to only combinational expression
- Targeted for dynamic checking only

# SV-AC Status

- Working document rev0.8 review started
- All working document sections reviewed
  - Issues resolution
    - Issues generated by 3 member votes
    - Proposals created and reviewed
    - Resolution by vote on proposals
    - 13 total issues, 11 resolved, 2 open
    - 2 new issues opened

# SV-AC Status

- Semantics working group started
  - Volunteer group of language experts to provide mathematical semantics
  - John Havlicek – Motorola - team leader
  - Roy Armoni – Intel, Cindy Eisner – IBM, Surrendra Dudani – SNPS
  - Semantics support expected by end of march

# SV-AC Future Plans

- Complete semantics effort
  - Complete semantic document
  - SystemVerilog 3.1 draft3 includes SVA. Will continue to enhance based on resolutions
- Complete work in SV-AC for v3.1 release by DAC
  - Synchronize with DWG changes
  - Resolve issues
  - Complete and publish SystemVerilog LRM
- Deferred enhancement could be considered for future release of SV LRM

# Milestones

| Milestone | Orig. | Actual |
|---|---|---|
| • Requirements approved | 9/27 | 10/3 |
| • OVA donation reviewed | 9/19 | 9/19 |
| • OVA donation vote | 9/30 | 10/3 |
| • First LRM draft | 12/1 | 1/21 |
| • Freeze new issues | 3/7 | |
| • All open issues resolved | 3/21 | |
| • Formal semantics complete | 3/31 | |
| • LRM vote by SV-AC | 4/30 | |

# Issues Going Forward

- Schedule
  - Close open issues
  - Multiple clocks is a major issue
- Synchronization
  - With rest of  SystemVerilog
  - FVTC