SystemVerilog Testbench Content

David Smith
Accellera SV-EC Chairman
Synopsys

Data Types

- Complete
  - String datatype plus operators and methods (dynamic size)
  - Enumerated type ranges and methods
    - first, last, next, prev, num,name
  - Class
  - Dynamic cast for handling cast problems

- In Review
  - Handle: used for declaring opaque handle for use with C Interface
    - handle foo;
  - Event: persistent state used for synchronization

Arrays

- Dynamic arrays with methods
  - new, size, delete
- Associative arrays
  - indexed by integer, string, class, signed packed array, unsigned packed array or packed struct.
  - Methods: num, delete, exists, first, last, next, prev

Aliasing

- alias
  - bi-directional short circuit within module
  - alias a = b;

Built-in methods

- Added concept of methods being attached to objects in the language for extension.
  - Use built-in method when applies to all data types or a specific data type
    - dynamic array.size or string.len
  - Parenthesis are optional on methods, functions, tasks, and built-in methods

Procedural

- Final block
  - Adds code that is executed at end of simulation without delays

```
final
    begin
        $display("Number of cycles executed %d", $time/period);
        $display("Final PC = %h", PC);
    end
```

Process

- Remove process keyword
- Added join_any and join_none to fork…join
- wait_fork for waiting that all child process end
- disable_fork to disable all child processes
- $suspend_thread to temporarily suspend the current thread.

Tasks and Functions

- Support void' to discard function return
  - void'(some_function());
- Pass by reference using "ref" attribute
  - subroutine(ref type argument);
- Default argument values
  - task read (int j =0; int k; int data = 1);
  - read(,5);
  - read(2,5);
  - read(,5,)
  - read(,5,7)
  - read(1,5,2)
  - read() or read is an error

Inter-process synch and comm

- Semaphores
- Mailboxes
- Persistent event (still in progress)

Clocking domain

- Specifies sampling and driving of verilog nets with respect to clock
- Supports skew for both sample and drive with respect to clock
- Supports “local” name of sampled or driven net

Program

- Container for procedural code related to testbench.
- Defines communication between design and testbench

Random Constraints

- Modification to class with rand, randc (cyclic), and constraint declarations

```
class Bus
    rand bit[15:0] addr;
    rand bit[31:0] data;
    contraint word_align {addr[1:0] == ‘2b0;}
endclass
```

- Adds randomize method to class to generate random values
- Other support as well.

Doubly Linked List

- Added as a class declaration (header)
- No implementation as part of the standard
- User must use “system” include to include header
- Limits keyword conflict