System Verilog Assertions v3.1

SV-AC update 2/28/2003

Faisal Haque – SVA-AC Chair
Stephen Meier – SV-AC Co-Chair

Agenda

- Constructs – agreed upon
- Open Issues
- Syntax Compatibility
- Extensions for Basic Committee

Constructs – Agreed Upon

- unary delay, binary delays, concatenation
  - semantics agreed, syntax open
- repetition
- boolean “throughout” a sequence
- sequence occurrence within a sequence
- implication – sequence implies a sequence
- top level properties
  - negation
  - always/initial
  - asynchronous reset
- directives – assert and cover

Open Issues

- dynamic variables during sequence evaluation
- always/initial syntax for directive/property specification
- multi-clock semantics
- delay (binary and unary) between sequences

Syntax Compatibility

- syntax of property/sequence definition
- usage/instantiations of definitions
- compatibility of syntax/semantics assertions in program block and verilog code

Extensions for Basic Committee

- “generate” feature to allow generating assertions
- new bit-vector functions in verilog expressions
- examine “template” feature for general applicability or future extension
- examine “bind” feature