SystemVerilog Basic Committee

Johny Srouji (Chair)
Karen Pieper (Co-Chair)

SV-BC: Status

- Charter
  - To address issues exposed in the SystemVerilog 3.0 standard through implementation
- Issues status
  - 283 issues have been filed
    - was 241
  - 228 (81%) have been addressed (8 are waiting on IEEE)
    - was 106 (44%)
  - 45 (16%) are actively being addressed
    - 16 have proposals and 29 are still active
  - 9 (3%) issues are delayed to next release
  - 0 are currently open

SV-BC: Schedule and deliverables

- Meeting schedules
  - Every two weeks for 2 hours
  - Several “BNF specific” meetings were held
  - Started using “email voting” to speed up resolving simpler issues, following an agreed-upon process

- Status
  - All changes up to 2/3/03 are reflected in 3.1 Draft 3
  - A microprocessor designer from Intel has joined our committee providing valuable “user aspect” feedback on System Verilog

SV-BC: Plans

- Based on SV 3.1 schedule:
  - April 1, 2003, Technology Freeze Date. Only clarification is allowed to be included in LRM. May 1 release to Board.
  - New issues must be filed by 3rd week of March
  - Will give higher priority to issues with proposals behind them