VCD data

SystemVerilog does not extend the VCD format. Some SystemVerilog types may be dumped into a standard VCD file by masquerading as a Verilog type. The following table lists the basic SystemVerilog types and their mapping to a Verilog type for VCD dumping.

SystemVerilog	Verilog	Size
bit	reg	Size of packed dimension
logic	reg	Size of packed dimension
int	integer	32
shortint	integer	16
longint	integer	64
shortreal	real	
char	reg	8
enum	integer	32

Packed arrays and structures are dumped as single vector of **reg**. Multiple packed array dimensions are collapsed into a single dimension.

If an **enum** declaration specifies a type, it is dumped as that type rather than the default shown above.

Unpacked structures appear as named **fork-join** blocks, and their member elements of the structure appear as the types above. Since named **fork-join** blocks with variable declarations are extremely rare, this will make structures easy to distinguish from variables declared in named **begin-end** blocks.

As in Verilog 2001, unpacked arrays and automatic variables are not dumped.

Note that the current VCD format does not indicate whether a variable has been declared as **signed** or **unsigned**.