

Replace "Section 12.6 Time unit and precision" with

SystemVerilog has a time unit and precision declaration which has the equivalent functionality of the ``timescale` compiler directive in Verilog-2001. Use of these declarations removes the file order dependencies problems with compiler directives. The time unit and precision can be declared by the `timeunit` and `timeprecision` keywords, respectively, and set to a time literal which must be a power of 10 units. For example:

```
timeunit 100ps;  
timeprecision 10fs;
```

There can be only one time unit and one time precision for any module or interface definition, or in `$root`. This will define a time scope. If specified, the `timeunit` and `timeprecision` declarations shall precede any other items in the current time scope. The `timeunit` and `timeprecision` declarations may be repeated as later items, but must match the previous declaration within the current time scope.

If a `timeunit` is not specified in the module or interface definition, then the time unit is determined using the following rules of precedence:

1. If the module or interface definition is nested, then the time unit is inherited from the enclosing module or interface.
2. Else, if a ``timescale` directive has been previously specified, then the time unit is set to the units of last ``timescale` directive.
3. Else, if the `$root` top level has a time unit, then the time unit is set to the time units of the root module.
4. Else, the default time unit is used.

The time unit of `$root` shall only be determined by a `timeunit` declaration, not a ``timescale` directive.

If a `timeprecision` is not specified in the current time scope, then the time precision is determined following the same precedence as with time units.