Minutes of SystemVerilog Meeting – 9/17/02

Attendance

Vassilios Gerousis (Infineon)
Dennis Brophy (Mentor Graphics)
Siamak Arya (Telairity)
Stephen Boyd (Boyd Technology)
Kevin Cameron (National Semiconductor)
K.C. Chen (Verplex)
Joe Daniels
Simon Davidmann (Synopsys)
Tom Fitzpatrick (Synopsys)
David Fong (S3 Graphics)
Harry Foster (Verplex)
Joao Geada (Synopsys)
Faisal Haque (Cisco)
Richard Ho (0-in)
Dave Kelf (Synopsys)
Ghassan Khoory (Synopsys)
Joseph Liu (Sun)
Erich Marschner (Cadence)
Grant Martin (Cadence)
Mike McNamara (Verisity)
Steve Meier (Synopsys)
Mehdi Mohtashemi (Synopsys)
Jayant Nagda (Synopsys)
Prakash Narain (Real Intent)
Darrel Parham (Sun)
Tarak Parikh (@HDL)
Karen Pieper (Synopsys)
Brad Pierce (Synopsys)
Rajeev Ranjan (Real Intent)
Ambar Sarkar (Paradigm Works)
David Smith (Synopsys)
Alec Stanculescu (Fintronic USA)
Stu Sutherland (Sutherland HDL)
Bassam Tabbara (Novas)
Kurt Takara (0-in)
Yatin Trivedi (The ASIC Group)

SystemVerilog Plans

- EM: What's NOT in the SystemVerilog charter?
  - SD: The vision is one language
  - EM: There must be some practical limit, such as Spice, etc.
  - VG: Some SystemVerilog enhancements may spill over to other committees
  - EM: Does the C/API level involve hw/sw tradeoffs, ie. some abstract level of design that can then be translated into hw or sw?
  - VG: No, things like that are tool issues.
- EM: Has any thought been given to making the 3.1 LRM align with the 1364 LRM?
  - VG: Having 1364 members in SV3.0 helped to keep things aligned.
  - EM: Will the 3.1 LRM modules be structured to fit into 1364?
  - VG: Copyrights are an issue.
  - EM: Can we get permission from IEEE to use their LRM as a reference.
  - VG: It will take a lot of effort to coordinate with IEEE, and I don't believe we'll have time. If someone can facilitate that coordination to meet our dates, then we can do it.
  - MM: An aggressive schedule would be to coordinate 3.1/3.0 aligned with 1364 by 2003/4. It may make sense to take 3.0 and edit it into a coherent

1364 document while 3.1 is continuing, and setting up some kind of coordination process.
    - VG: Ideas have been floated, but discussions have not started in earnest.
    - SB: When items go through 1364, they will be re-analyzed, not just rubber stamped.
    - EM: If SV3.1 is aligned with the 1364 LRM, then it makes it more obvious where the holes are.
    - SB: The 1364 members on SV3.0 have been vigilant in identifying these holes.
    - SS: The overall definition of the language is the BNF. SV3.0 did take the 1364 BNF and add to it, and SV3.1 will continue with that, and that is what will be handed back to 1364, so the BNF definition will be consistent.
- AS: Are there different categories of donation acceptance?
    - DS: Accept the donation, and modify it as committee sees fit.
    - VG: Acceptance of donation does not mean rubber-stamp of the donation going into 3.1.
- EM: There is some confusion over the status of the 3 FVTC languages that were not used as the basis for PSL. We need to clarify this.
    - MM,VG have a different understanding of the process from Erich's
- PSL Synchronization directives
    - SD: One important piece of language design is style. Is there a directive for style compatability with Verilog?
    - EM: The DWG is already considering style as a requirement.
    - FH: What are the priorities of the directives?
    - VG: The priorities are up to the committee.
    - SD: OVL insertion anywhere in Verilog means that OVL has to change from being a module library.
    - EM: By the time OVL capability can be fit anywhere in Verilog, will it still be a library, or will it be part of the language?
    - VG: It is important to keep a library of standard higher-level assertion functions, and this is what is required.
- SB: Given the milestones, should the EC committee start to consider items based on whether they can be completed in time? Will they be done in 3.2 or will they just be left off?
    - VG: It is up to the Accellera board to determine if there will be a 3.2. 3.1 will be donated to IEEE.
    - SB: A concern that there will be a lot of work being done in 3.1 that may not make it back to IEEE.
    - VG: We will have to have a discussion with the board whether there will be a 3.2. It is important for committees to determine for themselves whether to recommend that there be a 3.2.
    - SS: DVCon is 2/24, so the 3/1 milestone is too late.

SV-BC Committee Update (Karen Pieper)

- EM: It sounds like there may be some overlap between BC and EC in regard to interfaces. It sounds like the "interface" meeting must also consider the similar issues that the EC is considering.

SV-EC Committee Update (David Smith)

- No Questions

SV-CC Committee Update (Yatin Trivedi)

- GM: How does the 9/15 deadline for donations affect the potential Cadence technology of VPI enhancements? Is it now moot?
    - YT: The date has passed for considering the donation. If the board makes an exception, then the donation could be considered.
    - YT: The committee will not invent anything new, but will only consider donations.
- AS: The Assertion API is for access to the assertions, not for specifying assertions?
    - YT: Correct.

SV-AC Committee Update (Faisal Haque)

- No Questions

SystemVerilog-BC Issues

- JG: How do proposals get communicated between committees?
    - DS: Member(s) of one committee may be asked to champion specific proposals in the committee to which the proposal gets passed.
- EM: How are we guaranteed to ensure completeness of features across the different subcommittees, especially given the schedule deadlines? Can we establish completeness/quality criteria?
    - DS: There are formal and informal methods to do this. It would be a challenge to establish formal methods. Clearly the donators are heavily engaged in the process, and these people are good resources to ensure completeness.
    - EM: The goal of being schedule driven is in conflict with the ideal of being quality driven. There is not a small group of people responsible for identifying completeness/quality issues. How can we establish quality metrics?
    - ASt: Whatever is not there and working clearly will be cut.
    - JG: There is limited bandwidth for the chairs to be the conduit between different committees.
    - JN: All the language architects are still involved in the committees. The chairs should consult with these architects.
    - SB: If features get dropped, the IEEE is willing to accept donations of incomplete features, not just what is in 3.1.

- MM: 3.1 must avoid doing a disservice to users. We need to limit ourselves to the things we know we can do correctly given the schedule.
- SS: If something is missed, it's not critical since it will all get passed to the 1364.
- DS: There will be companies trying to implement 3.1. The better job we do now, the less pain the customers will see.
- VG: We are only accepting donations of working technology.
- EM: We're also modifying the donations. Should we come up with some sort of checklist to establish the criteria?
- VG: Getting early drafts of the 3.1 LRM out to the full committee will help people to identify such issues.
- EM: Suggestion that the chairs should do a "what could go wrong" analysis as issues come up.
- SB: When the full document is available, then it can be reviewed.
- EM: That is too late in the process.
- MM: The last months are a terrible time as last-minute stuff comes up between committees. This has to be started early.
- ASt: This problem can be contained by minimizing changes to the donations.
- EM: Will volunteer to be the repository of this list.
- **VG: The chairs will come back with a proposal on how to be pro-active to identify these issues.**
- VG: Issues that get raised based on actual implementation efforts will be given highest priority.

VeraLite Donation Review

- FH: Constraints were not mentioned, and it needs to be
  - MM: Constraints are not part of the donation
  - SM: Which committee will address constraints? Should be AC
- ASt: There are several other efforts that want to operate after NBA.
  - This is one of the issues that needs to be resolved across the different committees.

OVA Donation Review

- MM: **Will OVA be modified to have a similar clock syntax to the testbench donation?**
  - SM: That's a key issue that crosses the two committees. We're pretty open to modifying things if required.
- YT: Is 'clock' a context-sensitive reserved word?
  - Yes. As long as they are context-sensitive, the effect will be minimal.
- MM: Verilog is currently LALR1, in which keywords are keywords throughout. We may not want to change to SystemVerilog having context-sensitive keywords.
- Slide 25: PSL next_e does not map to OVA first_match. There is no PSL equivalent of first_match.
- Slide 26: PSL can support negative interrupt similar to how it supports length.

- MM: How does OVA compare to ForSpec?
    - SM: OVA2.0 and ForSpec2.0 are pretty much the same.
- RH: How will this subset of PSL/OVA be resolved with standalone PSL in Accellera?
    - TF: The PSL superset should be compatible with the SystemVerilog subset.
    - GM: How do you define the difference between SystemVerilog assertions and PSL from a tool-value perspective?
    - MM: The real advantage is that expressions written in one can be read by users of the other.
    - JG: It is a high priority for this group and for Accellera to come out with a statement to allay the fears/confusions of the user community.
    - VG: There is time to modify PSL before it gets approved as a standard.
    - EM: There is another group, the FVTC, that must also be convinced.

C-API Donation Review

- EM: We should do the SystemVerilog-calling-C side (DirectC) first, and then worry about C-to-SystemVerilog (cmodules) later.
- KC: Having new constructs in C (like '@') could have significant implementation issues.
- AS: **If the Assertion API has a method to find the assertion name, there may be overlap with the SV-AC requirement about whether assertions must be named.**
- **SystemVerilog Testbench should have the same capabilities as the assertion API for reacting to assertions starting/stopping/etc.**
- GM: The C-API group should discuss the usefulness of the coverage API before rushing to standardize on something with unclear semantics.
- MM: This is an API to ask "what's the coverage," where the definition may vary depending on what the tool can do.
- YT: The CC is soliciting requirements prior to voting whether to accept the donation. The CC is not proposing to standardize on a coverage tool, only an API.

Wrap-Up

- **EM: There seems to be overlap between committees w.r.t the type system**
- **DS: There are at least four different types of modules.**

Action Items

- Chairs will come up with a proposal on how to proactively identify quality issues that must be addressed.
- No proposals for additional features will be accepted after 9/30.
- Erich to send set of questions to sv-ec related to VeraLite donation
- AC/EC: Identify additional SystemVerilog testbench requirements for tb to react to or interact with assertions.
- Ensure that everyone gets a copy of the slides.

    - All presenters to send slides to VG.
    - Will be put on the website.
- Chairs: Need a process to examine language feature overlap orthogonal to the four committees.
- Single web page to hold cross-committee items (and links to other pages).