SystemVerilog Committee Meeting (Let Us Roll)

Vassilios Gerousis
Accellera Technical Chairman
Infineon Technologies

Agenda

- **SV Plans. 9:30 - 10:30 AM**
  - *Organization, Synchronization, LRM development and Milestones, SV policy and procedure.*
- **SV Committees Status 10:30 am - 11:10 am**
  - *Karen Piper --- sv-bc. (10 minutes)*
  - *David Smith --- sv-ec. (10 minutes)*
  - *Yatin Trivedi --- sv-cc. (10 minutes)*
  - *Faisal Haque --- sv-ac. (10 minutes)*
- **Break 11:10 - 11:15**
- **Enhancement/BC List and owners. 11:15 -12:00**
- **SV 3.1 TCC vision 12:00 PM - 12:30 PM**
- **Presentation of SV 3.1 donations: 12:30 - 3:40 PM**
  - *TESTBENCH. 12:40 - 1:40 PM*
  - *OVA 1:40 PM - 2:40 PM.*
- **BREAK 2:40 PM - 2:45 PM**
  - *C and API INTERFACE. 2:45 - 3:45*
- **Feedback on the donations: 3:45 PM - 4:00 PM**
- **Action items and conclusions. 4:00 PM - 5:00 PM**

SV 3.1 PLANS

SV CHAIRS

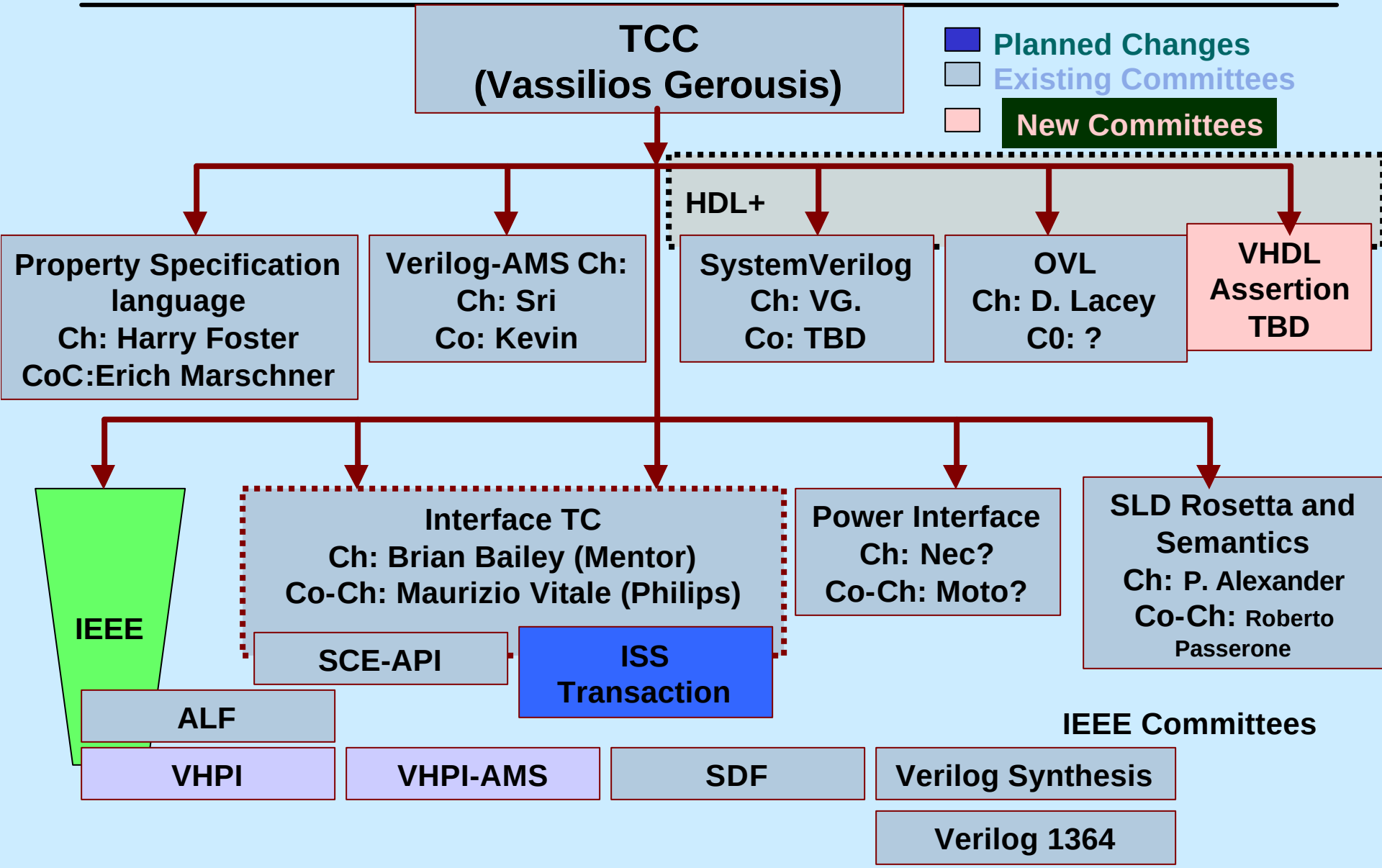
HDL+ Charter

- Advanced HDL languages into **higher design** abstraction and **advanced verification.**
  - Our focus is on extending current HDL languages.
  - We have started with SystemVerilog 3.0
- SystemVerilog 3.1 will be the first to accomplish this charter in the well proven Accellera two-step standard development.
  - SystemVerilog 3.0 is the first step. Many EDA vendors and users have started implementation of SystemVerilog 3.0.
  - We have seen the first feedback from Intel on implementation issues with SystemVerilog (and also IEEE 2001 Verilog).

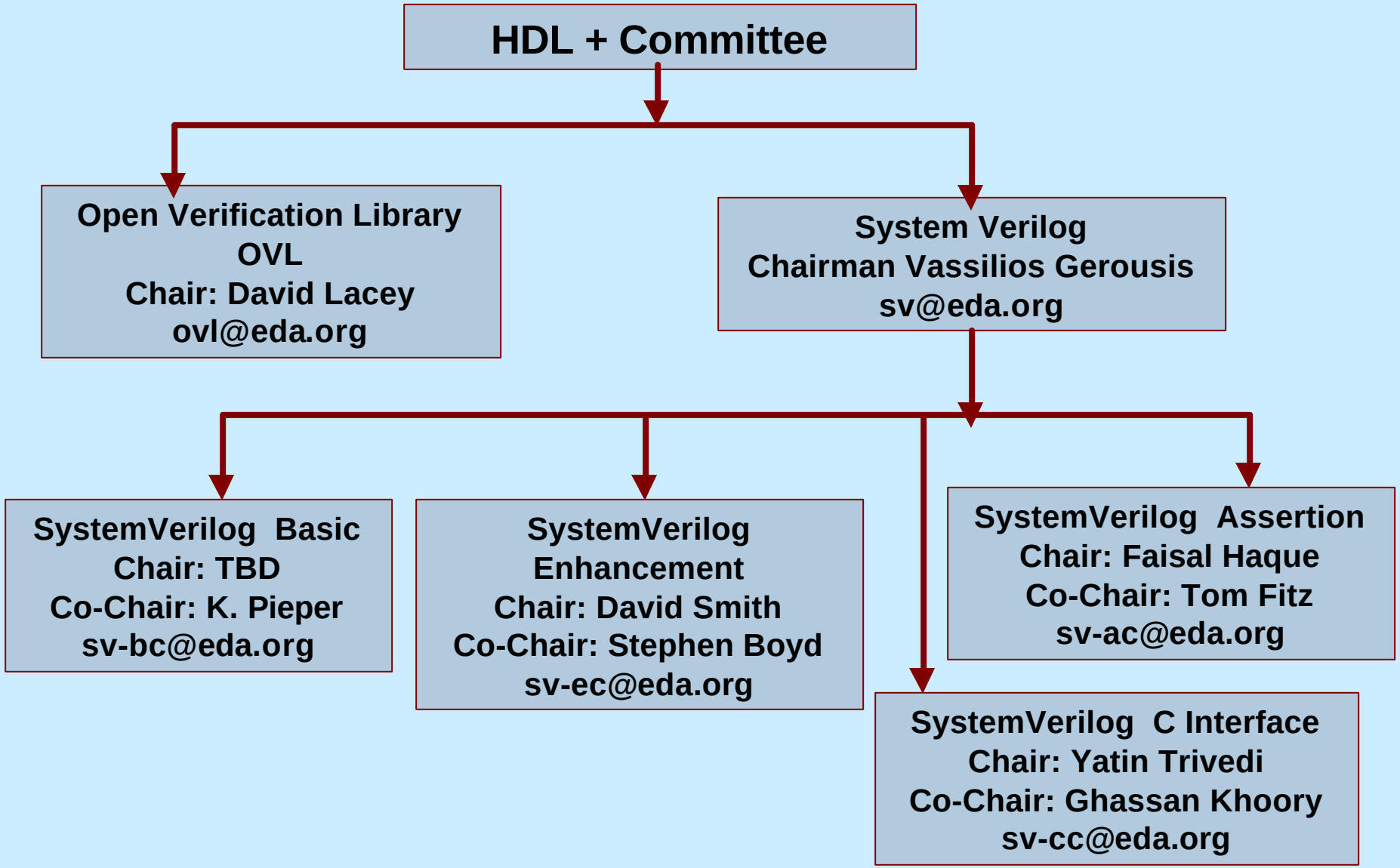
SystemVerilog Charter

- **Charter:** Extend Verilog IEEE2001 to higher abstraction levels for Architectural and Algorithmic *Design* , and *Advanced Verification*.
  - **Design Abstraction:** Interface semantics, data types, abstract operators and expressions extend the efficiency of Verilog into architectural design space.
  - **Verilog assertions** provides advanced verification capability for **semiformal and formal** methods (formal, simulation and hybrid).
  - **Testbench and Coverage Enhancement** add needed enhancement for simulation and hybrid verification
  - **C and API interface**: Direct C interface enable co-design and third party implementation.

Accellera Technical Committees



HDL+ Committees



SV Committees Status

- *Karen Piper --- sv-bc. (10 minutes)*
- *David Smith --- sv-ec. (10 minutes)*
- *Yatin Trivedi --- sv-cc. (10 minutes)*
- *Faisal Haque --- sv-ac. (10 minutes)*

SystemVerilog Basic Committee

Chair to be determined

Karen Pieper, Co-Chair

SystemVerilog Basic Committee

- 143 issues currently with more expected
  - 38 are complete
    - Not an issue
    - Handed off to another committee
    - New wording proposed
- Interfaces appears to be the most contentious issue
- Completion in February
  - Assuming 200 total issues are filed
  - Assuming a passing rate of 20 per meeting
    - More than 50 of the remaining issues have proposals
  - Assuming a special meeting on Interfaces

SystemVerilog Basic Committee

- Process is to discuss each issue
  - Determine
    - > If it is a real issue
    - > If it belongs somewhere else
    - > Has an acceptable proposed fix
      - – Vote on proposal
    - > Requires further explanation of the functionality
      - – Creates an action item to clarify functionality and make a proposal for new wording

SV-EC Status
17 September 2002

David Smith – Chairman

Stefen Boyd – Co-Chairman

Agenda

- Mission
- Process
- Milestones
- Status
- Challenges

Mission

- Process any donations provided to the committee by the TCC chair – Synopsys Testbench donation
- Extend the Verilog language to system design and for testbench using a single syntax

Process - Donation

- Review all 8 chapters of donation. Purpose is to analyze and evaluate donation. During review develop list of issues organized by:
  - a. missing information
  - b. inconsistent information within donation
  - c. conflicts with Verilog/System Verilog (both syntax and semantics)
  - d. items to be migrated to System Verilog
- Resolve issues in categories a and b.
- Vote on acceptance or rejection of the donation
- Resolve issues in category c and migrate issues in category d to extension list (as appropriate)
- Create LRM based on initial donation that follows the IEEE Verilog style including BNF
- Committee votes on overall LRM to submit to parent committee/board

Process - Extensions

- Originally 12 items for extension (Rated and propose)
  - Alias
  - Process control
  - Data channels
  - FSM
  - Extern Modules
  - Inferred Reg Type
  - Multi-clock/Hier. FSM
  - Data Path
  - OO
  - Force/release with strengths
  - Pointers
  - OO

Alias (Cliff/Kevin)

Process Control (Kevin)

Data Channels (Kevin)

FSM (Cliff)

Extern Modules (Alex)

Inferred Reg. Type (Cliff/Kevin)

Process – LRM

- Resolve Donation Open Issues list (18)
- Create LRM team
  - Create LRM for purpose of deciding what is to be included
  - 3 experts (tech writing, VeraLite, System Verilog)
  - Document current donation plus clarification
  - Input from committee as items resolved
  - Committee reviews and approves

Milestones

- 8 July – 19 August review as much of Donation as possible.
- 4 September – Full day meeting on Clarifications
- 15 September – Approve donation and close acceptance of new donations and proposals for 3.1
- 30 September – LRM outline with donation mapping
- 14 October – Start review of modifications to existing LRM sections
- 28 October – Start review of modifications to new LRM sections
- 1 March – Complete review of LRM based on donation and extensions

Status

- First pass review of technical content is complete
- Donation approved
- LRM committee in formation
- Initial proposals for top 3 priority extensions

Challenges

- Completing work on existing extensions
- Likelihood of having to work on other extensions
- Aggressive LRM schedule
- Keeping momentum on testbench issues

SystemVerilog
Assertions Committee
SV-AC

Faisal Haque
SV-AC Chair
Cisco Systems

Status

- Formed Working Group (DWG) to develop a draft of LRM
  - Six people group
  - Selected for ability to contribute
- Requirements being reviewed
  - Vote expected on 9/27

Process

- Requirements
- Create a common subset of OVA and PSL
- Merge with DAS 1.0 subset
- Draft LRM reviewed and approved by SV-AC

Milestones

- Requirements Approved 9/27
- First LRM Draft 12/1
- Approved by SV-AC 3/1

SystemVerilog Committee Meeting

Status Update
SV-CC

Yatin Trivedi

Ghassan Khoory

SV-CC Charter

- Provide foreign language interface to SystemVerilog.

- Work with proposals donated to Accellera
- Analyze and establish requirements of SV API
- Enhance Verilog APIs to support SV
  - Direct C/C++ access
  - Assertions
  - Coverage
  - VPI

Members

- **EDA Vendors**

Francoise Martinolle	Cadence
Stuart Swan	Cadence
Simon Davidmann	Co-Design/Synopsys
Peter Flake	Co-Design/Synopsys
Bassam Tabbara	Novas
Joao Geada	Synopsys
Ghassan Khoory	Synopsys
Andrzej Litwiniuk	Synopsys

- **Users**

Michael Rohleder	Motorola
Kevin Cameron	National Semiconductor
Darrell Parham	Sun Microsystems
Alain Raynaud	Tensilica
Yatin Trivedi	The ASIC Group

Members

- **Observers**

Tarak Parikh	@HDL
Vassilios Gerousis	Infineon
Josef Derner	Mentor
Karen Bartleson	Synopsys
Michael McNamara	Verisity
K Chen	Verplex
DRM	Xilinx

- Active participation
- Issues discussed on reflector
- Reflector sv-cc@eda.org

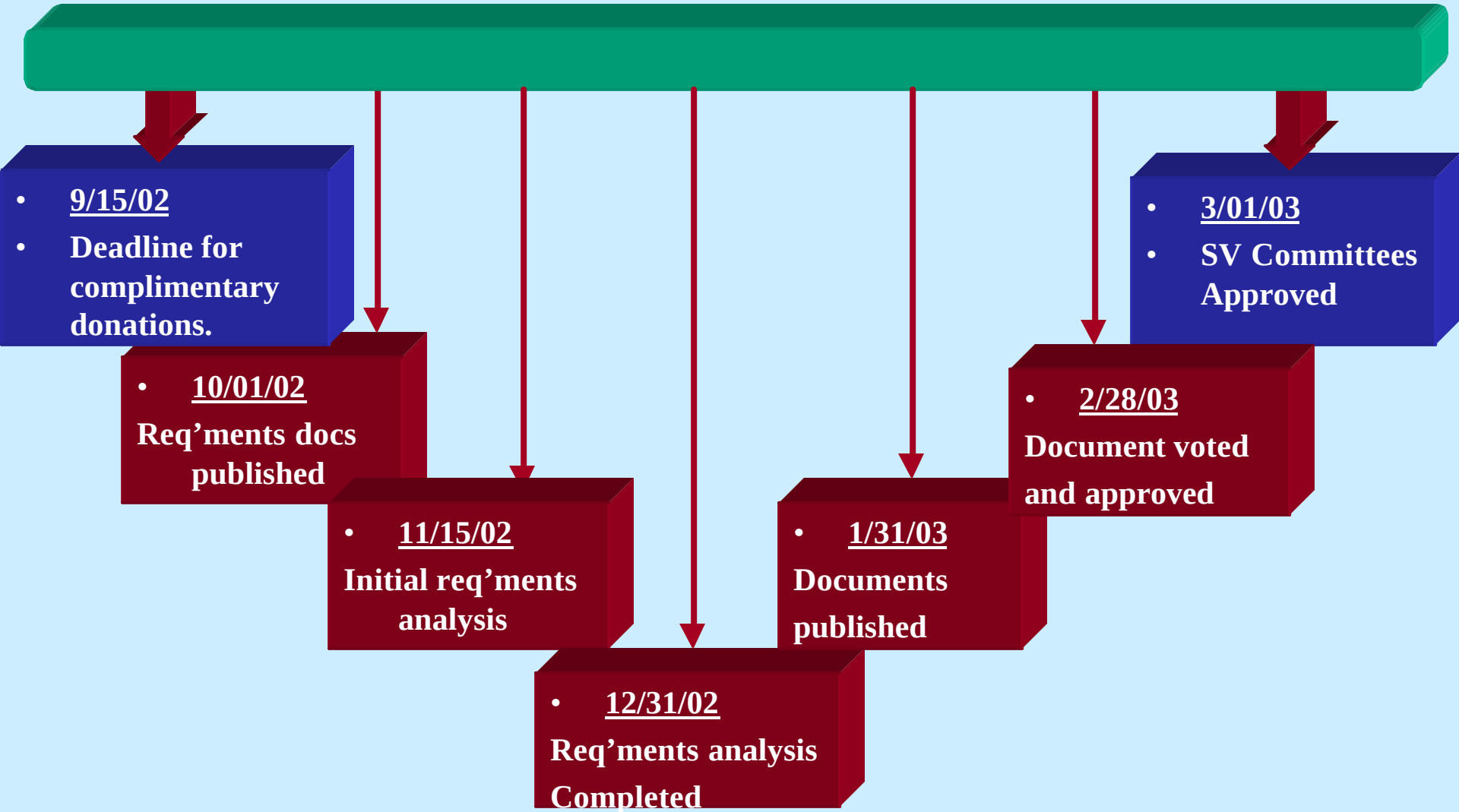
Progress Report

- Work in 4 areas
  - Direct C/C++ API
  - Assertion API
  - Coverage API
  - VPI Enhancements
- Direct C, Assertion and Coverage proposals donated by Synopsys
- VPI is expected from Cadence
- Conference Call every 2 weeks

LRM Development

- Requirements documents
  - Global
  - Direct C
  - Assertion
  - Coverage
- Expecting VPI requirements and proposal
- Map requirements to proposal (donation review)
  - Proposal meets requirements
  - Proposal partially meets requirements
  - Proposal conflicts with requirements
  - Proposal does not address some of the requirements

SV-CC Timeline



Realistic Timeline

	Req'ment Document	Proposal Review	Document Published	Document Voting
Direct C	10/01/02	11/15/02	11/30/02	12/15/02
Assertion	10/01/02	11/15/02	11/30/02	12/15/02
Coverage	10/15/02	12/15/02	12/31/02	01/15/03
VPI	10/15/02	12/31/02	01/15/03	01/31/03

- Individual item (e.g. section, chapter) voting will be part of proposal review process. Once all issues are resolved, final document will be published and voted for SV-CC approval.
- Discussions and voting will be concurrent between 4 reviews on email reflector.

MOVING AHEAD

LRM Development

- We will have one LRM for SV 3.1.
- The primary SV 3.1 editor is Stuart Sutherland.
  - Yatin will help Stuart to edit C / API portion.
- Stuart can focus on immediate job for the basic committee and provide assistance to other SV committees.
- Stuart will work directly with the SV chairs during the LRM development:
  - Planning: Organization and contents.
  - Assembly: Adding modules to SV 3.0 LRM.
  - Modification: Modification of SV 3.1 RLM.
  - Final release: Clarification and corrections

SystemVerilog 3.1 Process Page 1

- Established 4 SV committees, Each is responsible for:
  - a- Technical content within their charter.
  - b- Implement interfaces or enhancement requested by the other committees.
- A joint committee is assembled (SV)
  - Review Progress.
  - Synchronize.
  - Review the assembled LRM. Partial assembly will be done.
- LRM Development And Synchronization:
  - a- Each committee will address the current available donated materials.
  - b- Each committee will vote to accept/reject donations. If portions are accepted. the donation is accepted.
  - C- Each committee will develop an LRM portion of the donated material.
  - d- Each committee will make available to the other committee any request to enhance certain capability required. (e.g. SV language constructs for using C model or task should be done ??)

SystemVerilog 3.1 Process Page 2

- e- Other committee must address the request with actions.
- f- Joint meeting if necessary should be done to address common agreement.

- Review and Voting:
  - a- Each committee develop and build an LRM portion.
  - B- Each committee allocate time to review and vote on final draft. (Exception is SV-AC).
  - C- A partial LRM is established as soon as materials have been accepted and voted by any committee.
  - d- A full LRM draft should be assembled as soon as all materials are ready.
  - e- Each committee will review their content "in context of the full LRM".
  - f- The full committee review the final draft of the LRM. Any changes, is sent back to the appropriate committee for modification.
  - g- When all issues are resolved by each of the committees the full committee then votes on sending the final draft of the LRM to the Accellera board.

SystemVerilog 3.1 Process Page 3

- SV chairs will steer organization and vision building for SystemVerilog.
  - Top level decisions to drive the SV 3.1 development.
  - First level of synchronization between the four committees.
  - Top level Milestones and schedule development.
- SV 3.0 Issues And Enhancement List: We have assembled an impressive list of enhancement and issues based on SystemVerilog 3.0 standard.
  - a- A deadline is set for end September to provide owners a final chance to submit a proposal. No proposal, by that date, will automatically remove that item from SystemVerilog 3.1 release.
  - b- Feedback on SV 3.0 implementation will be added to the list automatically and given the highest priority for resolution.
  - c- SV 3.0 issues list and enhancement will be closed at the end of December.
  - d- Feedback on SV 3.0 implementation will continue until the final draft is completed and voted on.

SV 3.1 Synchronization

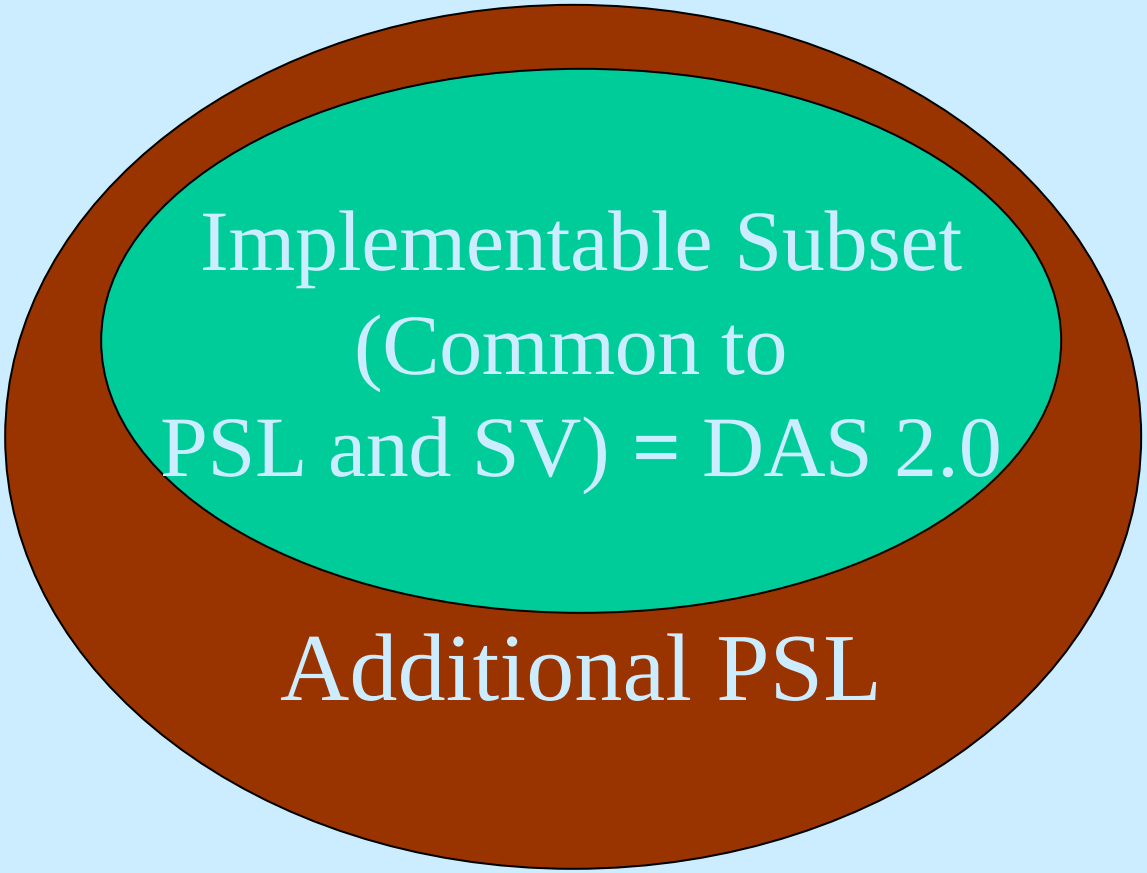
- First Layer
- Second Layer
- Third Layer
- Fourth Layer

- Enable formal communication in all layers.
- Disconnects must be resolved in all layers.
- Synchronization directives, using SV chair vision should be used as basis to build SV 3.1.
- Joint committee meeting is encouraged.
- Every member has the responsibility to make synchronization work.

Synchronization with PSL

- We have created a language working group in the assertion to focus on unified assertions.
- The language group has agreed to use the common set between OVA and PSL and create an SV assertion DAS 2.0.
- The SV chairs directive is to ensure:
  - Compatibility with Verilog language (semantics and syntax).
  - One SystemVerilog BNF.
  - OVL insertion anywhere inside Verilog.
  - Implementation (simulation, current formal technology and hybrid) for both intelligent verification and synthesis.
  - One Style.

Implementable Subset



- **We have duty to make sure this happen.**
- **Use future PSL to add to newer version of SV (e.g 3.2)**

SV 3.1 Milestones

- Target Date: DAC 2003 for delivering Accellera Standard 3.1 for SystemVerilog.
- May 1 deliver Final LRM draft voted by SV committee to Accellera board. We have given Accellera board one month to review and vote formally.
- March 1: Completed LRM draft (each committee deliver agreed and voted portion of the LRM).
- LRM review period for SV, and allow corrections is two months March 1 to May 1.
- Last Modification date is April 1 of technology. Between April 1 and May1, is just to do clarification.
- First assembled LRM is planned for End of October. (it can be partial based on accomplishment).
- LRM draft for distribution at HDLCON (renamed to DEVCON) is March 2003.

SV 3.1 Milestone

- **September 15 2002**
- Deadline for complimentary donations.

- **October 31, 2002**
- First Assembly of 3.1 LRM

- **February 24, 2003 DEVCON**
- SV Committees Approved
- Public Release Of SV 3.1

- **June 2003 DAC**
- SV 3.1 Standard

- **September 30, 2003.**
  - Finalize enhancement list
  - No proposal means automatic removal from 3.1.
  - Vote for acceptance of donations.

- **April 1, 2003.**
  - Technology Freeze Date.
  - Only clarification is allowed to be include in LRM.
- May 1 release to Board.

Enhancement And Issue List

Please act for progress

- Issue List (Basic Language):
  - Progress is being achieved.
  - Implementation improvement: Intel is ahead of the pack in providing real feedback.
  - We must encourage more implementation feedback.
- Enhancement List:
  - Kevin seems to be the only one who is providing proposals.
  - Deadline is imposed. No proposals will be accepted after September 30, 2002.
  - All proposals provided, is automatically become the ownership of Accellera.
  - Please do not submit any patented materials.

SV VISION

SystemVerilog Plans

- Improvement based on SV 3.0 tool implementation
- Direct C/C++, SV API, Coverage API, Assertion API.
- Improved assertions (Common set of OVA and PSL)
- Testbench
- Improve HW/SW co-design.
- Improved Language for algorithmic/architecture.

IEEE

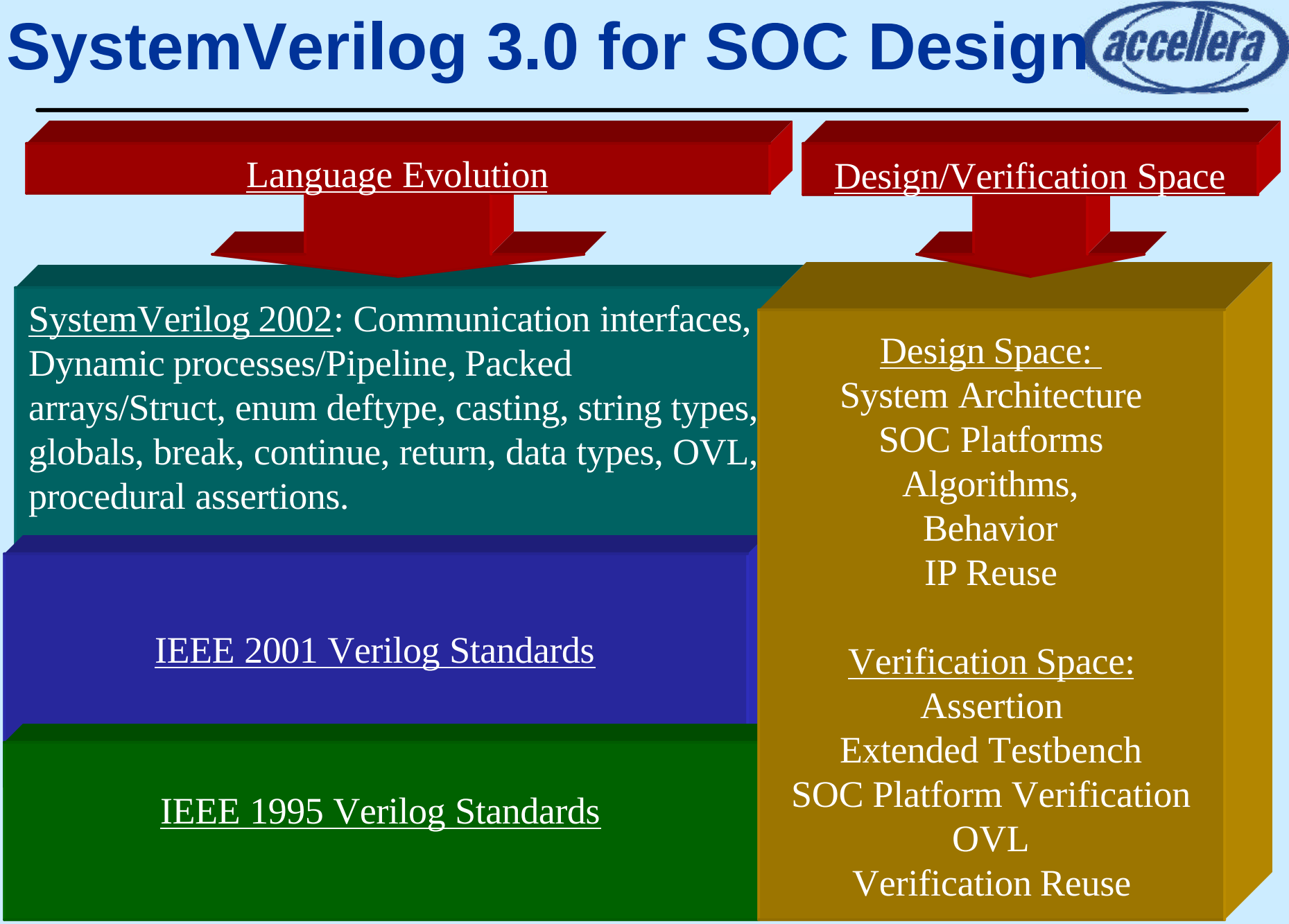
SV 3.1 DAC2003

SystemVerilog

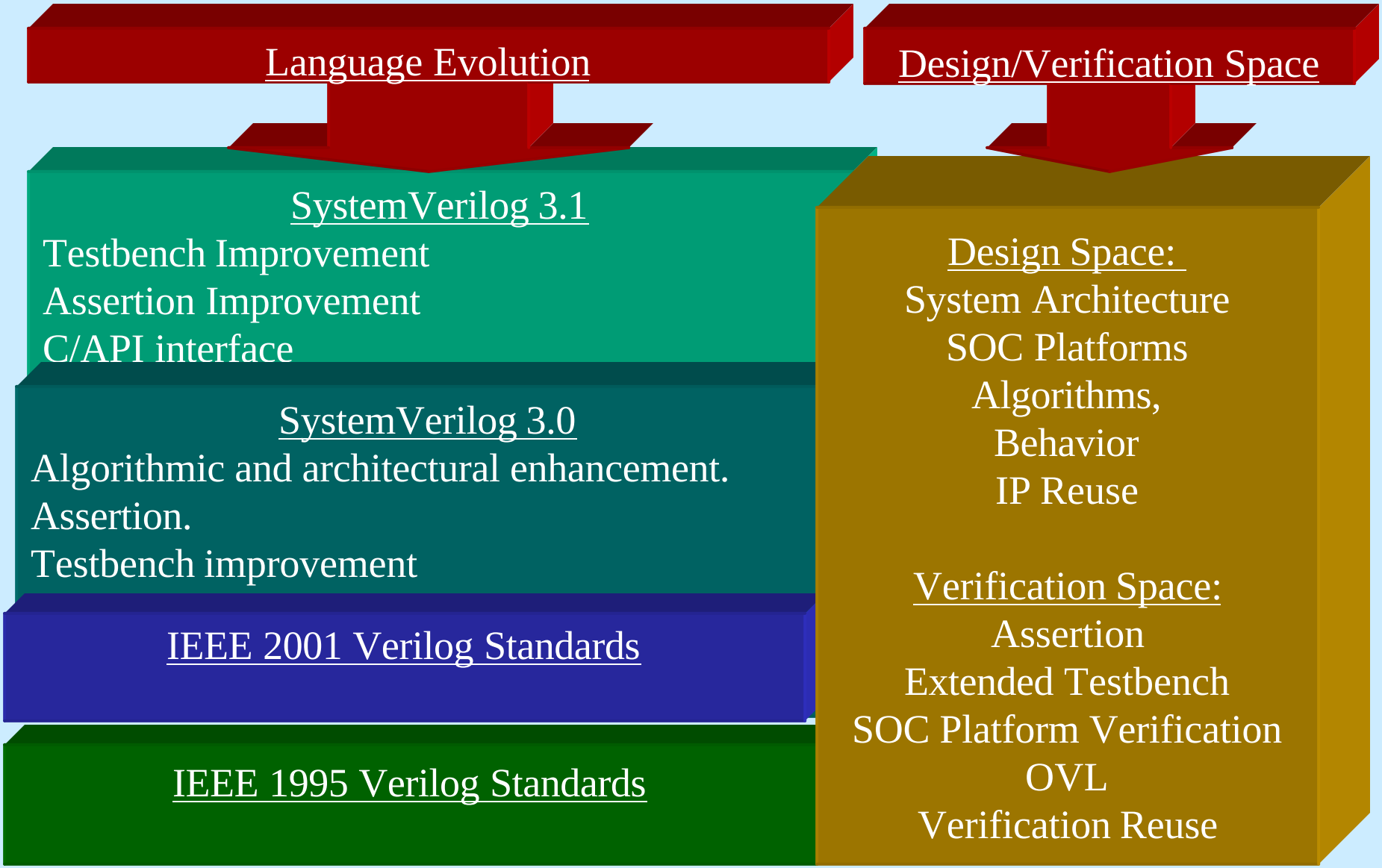
SV 3.0 DAC2002

- Architecural Language.
- Introduces Assertions.
- High Level Assertion Library (OVL).
- Interface-Based Design.
- High level constructs and data types.
- Algorithmic language.

SystemVerilog 3.0 for SOC Design



SystemVerilog 3.1 - Smart HDVL



Conferences

- FDL 2002 (SV, PSL, Rosetta).
- DVCON 24
  - SV 3.1 tutorials.
  - LRM Draft.
- Presentation by all chairs:
  - US.
  - Japan.
  - Europe (Date 2003).
- DAC 2003

Next

- Partial LRM.
  - Stu and SV chairs to work out a plan.
- SV meeting (face to face November).
- What happens after 3.1 (will discuss with SV, IEEE 1364, and Accellera.).
  - 3.1 is targeted for IEEE.
  - 3.2 extensions (3.1 implemention and possible donations).