



Unified Power Format
Technical SubCommittee
UPF-TSC

13 September 2006

Stephen Bailey
Chair

Agenda

- 8:30 Welcome & introductions
Stephen Bailey
- 8:45 Review UPF-TSC project proposal
David Peterman
- 9:15 Update on upcoming Low Power Workshop
Kevin Kranen and Sumit DasGupta
- 9:45 Break
- 10:00 Available Technology for standards development
Various
- 12:00: Lunch break
- 13:00: Available Technology for standards development
various
- 14:00 Standards development process
- 14:15 Break
- 14:30 UPF-TSC Organization
- 15:45 Next meeting(s)
- 16:00 Adjournment



Welcome & Introductions

- Accellera contacts
 - Chair: Shrenik Mehta, Sun
 - TC Chair: Johnny Srouji, IBM
 - TSC Chair: Stephen Bailey, Mentor
 - TSC Vice Chair: TBD
- Attendee introductions





Review UPF-TSC Project Proposal

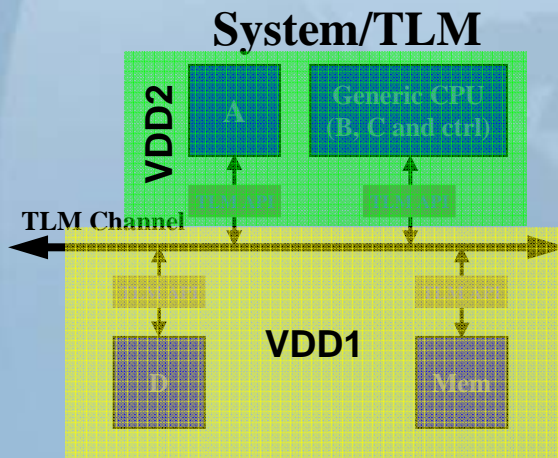
David Peterman

Industry Need

- Power has become the dominate factor in the design of today's electronic systems
 - Explosion in battery operated systems
 - Many (most) non-portable designs are also constrained by power consumption requirements
 - Heat generation and dissipation
 - Practical power supply & management
- Current state is a hodge-podge of commercial and ad hoc solutions
 - SAIF, GAF, etc.
 - Specification of power aware design characteristics
 - Often done late at gate-level and ad hoc
 - Need to verify correctness of power-aware functionality
 - Done sooner and with higher correlation to design intent

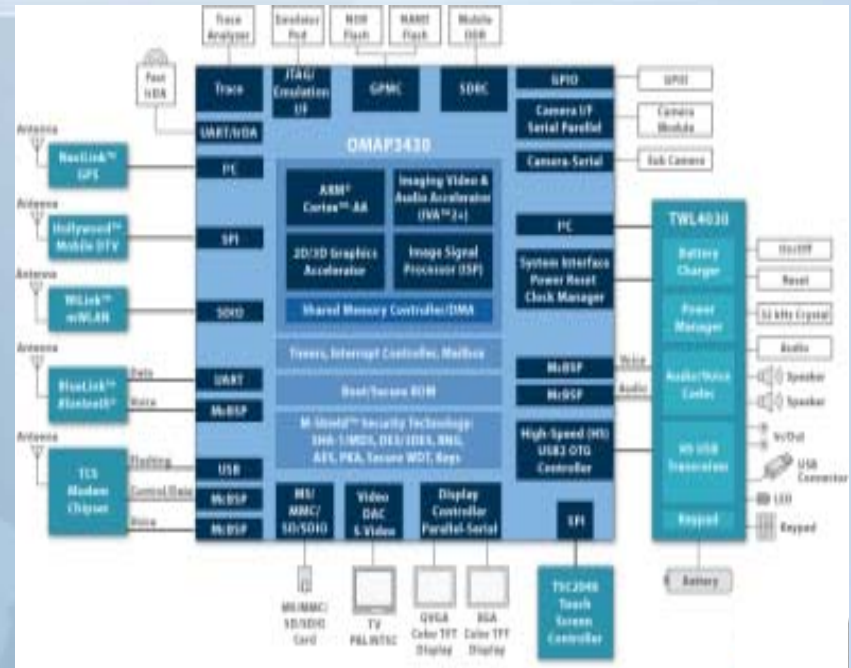
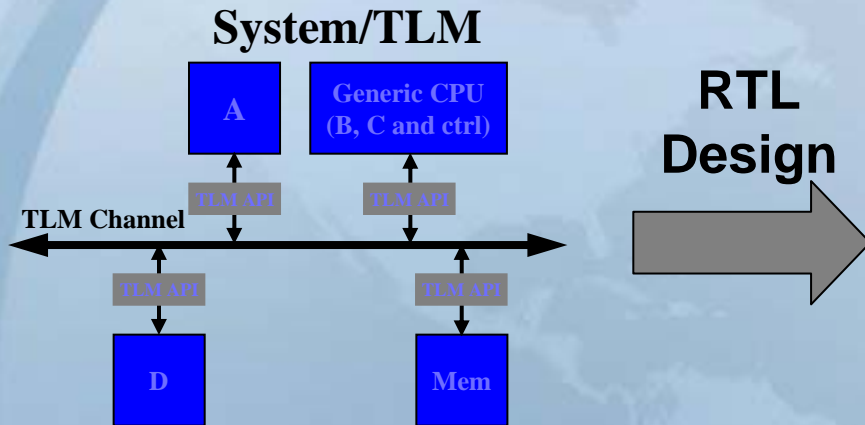


Low Power Design Overview



- At System/TLM level:
 - Experiment with power island and voltage domain layouts
 - Budget dynamic power
 - Estimate dynamic power usage
 - TLM power management functionality
 - Identification of state save and restoration requirements
- Standardization areas:
 - IP:
 - State save/restore
 - Operating voltage(s)
 - Power aware design, verification & estimation/analysis specification

Low Power Design Overview (2)

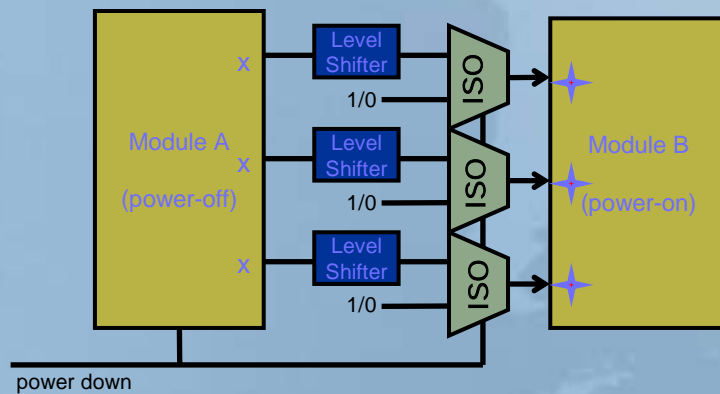
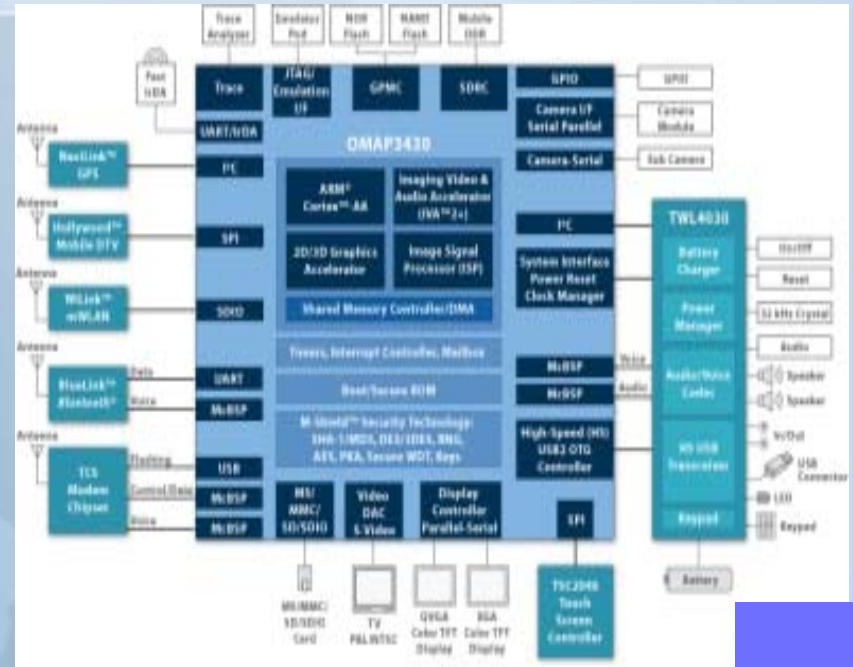
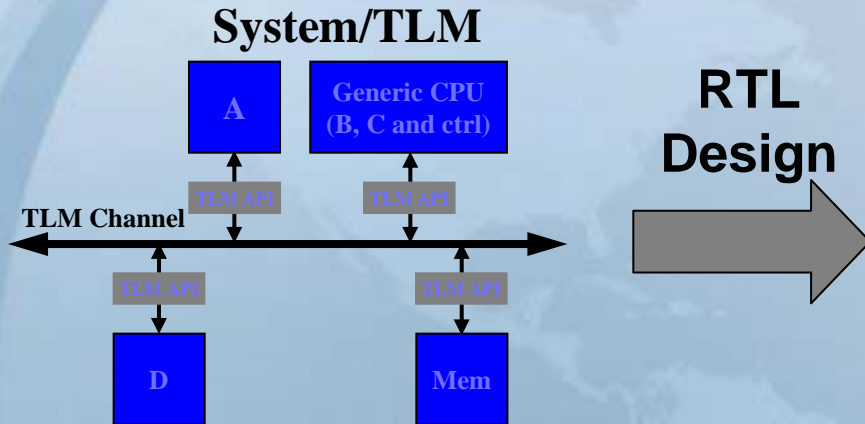


- Power-aware design characteristics

- VDDs, power islands, isolation, retention, constraints
- Specification for use in:
 - Functional verification – level shifters between VDDs, correct functionality in power down, up or reduced voltage modes
 - Directing synthesis to meet constraints and insert power-aware functionality (isolation cells, retention flops/latches)
- Analysis: Dynamic power consumption estimation



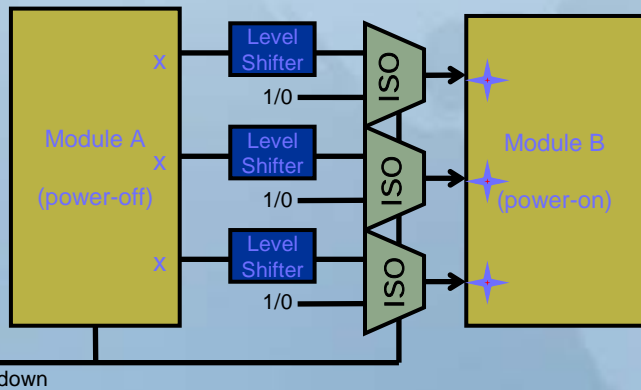
Low Power Design Overview (3)



Gate Implementation



Low Power Design Overview (4)



**Gate
Implementation**

- Gate implementation
 - Power aware (retention, isolation) behavior matches RTL verified behavior
 - Equivalence checking of RTL vs. Gate
 - Dynamic power calculation

Low Power Design Overview (5)

- Physical implementation & verification
 - Static power consumption (leakage)
 - Accurate characterization of dynamic power consumption parameters for cells



Why Standardization

- Portability of power aware design information
 - Portable across tools in the flow
 - TLM, RTL, Gate design capture & verification
 - RTL-Gate equivalency checking
 - Dynamic (simulation) and static (linting and formal) verification
 - Could be HDL enhancements, “side files” or both
 - Power consumption estimation and synthesis constraints/budgets
 - Across competing tools
 - Not locked into a single vendor solution
 - That may be limited to a subset of the overall flow
- IP Reusability in low power designs
- Library standards
 - Modeling
 - Easy integration into designs
 - Use in verification
 - Parameterization and characterization
 - Use in implementation (synthesis)
 - Accurate calculations
 - Physical verification



Demonstrated Need

- DAC 2006:
 - TI and Nokia organized a meeting on the topic of an open standard for low power design flows
 - The 4 top EDA vendors attended
 - Plus Atrenta
 - Broad, significant user representation including
 - TI
 - Nokia
 - ARM
 - ST
 - Philips
 - Sun
 - Shrenik Mehta represented Accellera



Mission of Accellera Low Power Flow TSC

- The accelerated development of an open, comprehensive standard for the specification of power-aware requirements, design intent and implementation, verification and analysis across all design abstraction levels.



Scope of UPF TSC

- Abstraction levels
 - Cover System (TLM), behavioral/algorithmic, RTL, gate, transistor and layout.
- Specification
 - Design requirements
 - Design constraints (hard and soft)
- Implementation
 - Specification design intent such as voltage domains and power islands and the related signal network
 - Intended power-aware functional behavior (e.g., retention)
- Verification
 - Semantic specification of how the requirement and design information can be used by verification tools as input to verify correctness of the power-aware characteristics of the design combined with the correctness of the design functionality
- Analysis
 - Specification of statically and dynamically relevant information that may be used for estimating and/or calculating power consumption, leakage and loads.
- Examples of low power information that are candidate for inclusion in the standardization effort:
 - Power-aware design data
 - Power-aware design constraints
 - Power-aware constructs for standard languages (including VHDL, Verilog, SystemVerilog, SystemC and IP Exact)
 - Power-aware library models
 - Power-aware circuit activity



Proposed Timeline

Week Of	Milestone
11 Sep 06	Accellera TSC formation
	Initial TSC Meeting
18 Sep 06	Design Objectives Document; Weekly meetings start
5 Oct 06	Si2 / Accellera Workshop on Low Power
30 Oct 06	First drafts available for review
30 Nov 06	Submission to Accellera Board for Approval
31 Jan 07	Hand-off to IEEE and/or other suitable standards organizations





Update on Upcoming Low Power
Workshop (5 October 2006)



Available Technology for UPF-TSC Consideration

Agenda – Available Technology

- 10:00 Synopsys – Jim Sproch
- 10:30 Mentor -- Stephen Bailey
- 11:00 Magma -- Yatin Trivedi
- 11:30 Rob Mains -- Sun
- 13:00 Vast Systems --Graham Hellestrand





Standards Development Process

Basics -- Accellera

- Accellera policies and procedures apply
 - Available on the web
http://www.accelera.org/activities/Accellera_TC_Policies_Procedures_V2.0.pdf
- Roberts Rules of Order for moderating and conducting meetings
- Open meetings
- Anyone can participate
- Only Accellera members can vote
 - “Polls” of participants may be taken
 - One vote per Accellera member



Accellera Approval

- Draft standard is distributed for review and comment
 - To all participants and Accellera board members
- Draft is submitted to Accellera board for approval
 - Majority approval required
 - Board typically provided 30 day review period



IEEE

- Accellera is recognized by the IEEE as a standards incubation/development organization
- Process to hand-off standards from Accellera to IEEE for IEEE standardization is well defined
 - IEEE working group (entity membership)
 - Specification handed over
 - IEEE WG may update the spec
 - “Errata” uncovered by early implementations
 - Cover functionality holes exposed by early adopters



Additional Possibilities

- Other standards organizations can be used if appropriate
 - Si2, for example



Additional Considerations

- Accellera and Si2 Cooperation and Coordination
 - Details under discussion
 - Possibilities
 - Architectural review & coordination, requirements
 - Validation
 - Reference implementations
 - Industry outreach
 - “Standards marketing”
 - 5 Oct 06 workshop
 - Follow-on events for education and awareness





UPF-TSC Organization

Scope Implies Organization

- Specification of design intent and constraints
 - System/TLM and RTL
 - Modeling guidelines/requirements
 - IP reuse
- Library formats
 - E.g., Liberty
- Analysis data formats
 - Estimation
- Each subgroup needs a technical leader
 - TSC serves as coordinator





Next Meetings

Weekly Meetings

- Telecons primarily
- Tuesdays?
 - 8am Pacific start
- Except 5 Oct 06
 - In-person 6 Oct 06 in Bay Area
 - Day after workshop
- Periodic in-person meeting – monthly?
 - Trying to schedule a meeting in Europe
 - Will target notice 3-4 weeks out for in-person



Telecons

- Administrative, general
- Technical discussions
 - General TSC meeting can adjourn
 - With remaining time used by subgroup(s) of TSC
- Next Meeting Tuesday 26 Sep via telecon



Infrastructure

- upf-tsc@accellera.org

