

Accellera Low-Power Workshop: User companies considerations

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17.04.2007

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Introduction

Past

- Power has been the 2nd priority for SoC Development
 - Designs have been optimized for Performance and Area
 - Power targets have been easy to meet.
- There has been only some tools supporting Power implementation and verification
 - No big business seen by EDA providers
 - No major development activities seen (Methodology or Tool)

Now

- Gate count explosion because of growing complexity and added features with increasing performance requirements have caused dynamic power consumption to multiply.
- Silicon technology progress (65 nm and beyond) enabling this gate count explosion has made leakage power a significant problem
- **Power has come as a major issue to solve for new devices**

Needs for standardization

- Power Management is everyone's concern to solve
 - There is need for co-operation to find best solutions for industry. It means effort from System houses, Silicon, IP and Tool providers
 - It means more viewpoints for issues: from system to libraries and from high level to tiny details
- Standard is enabler for building fluent flow and Methodology
 - Same agreed terms for everyone
 - General methodologies developed around it
 - Tools interoperability ensured
 - It gives opportunities for inventions (Tools and Methodologies)
 - By having standards for today's needs we can concentrate for tomorrow's issues
- On-going standardization effort in several bodies should be avoided. It means incoherence and wasted resourcing for whole industry
 - Standards development should be **Quick, Open** and **Inclusive**
 - No standard is bullet proof, but industry wide standards are cleanest

Nokia Requirements for Power Management Flow

- **MISS a KISS**

- **Make It Simple Silly and Keep It Simple Stupid**
- Improvement definitely needed for PM Configurations

- **Usability**

- Completes existing flows, doesn't break it.
 - For users learning curves easy for deploy.
- Not enormous setups and new skills needed

- **Portability**

- Platform based design style supported: IP and SoC level activities not conflicting.
- Deliverables from IP level is including information how to implement and verify Power Management for IP when integrated to SoC

- **Reusability**

- For derivate designs 20% to be done (not vice versa).

- **Tool interoperability**

- No scripting needed for having tools to work together

Nokia Requirements for Power Management Flow

- **Verification automation**

- There is need to automate verification for having PM implementation first time right

- **Methodology**

- Based on lessons learnt in industry there is need for Methodology definition:
 - How to implement, verify and still survive from Power Management.

- **Solution in Phases**

- **1st Phase:** Solve first RTL downto GDSII flow.
 - Implementation, Verification, DFT
- **2nd Phase:** Increment solution to ESL.

UPF Standardization Activity

- Accellera's effort for making industry wide power format standard has been unique
 - Quick: UPF TC Founded Sep 12th 2006, UPF1.0 approved Feb 28th 2007
 - Standard was made from scratch within 6 Months
 - Open: No NDA's were needed, Free to everyone use
 - Inclusive: Everyone one can participate
 - Many donations given by EDA and User companies
 - Technical events in US and Europe
 - Weekly Telecons
 - Active participation from whole industry
- Nokia is committed to use UPF standard in SoC production flow
 - UPF support from EDA industry is required for H2/2007

Summary

- Finding Power Management Flow for SoC design is everyone's interest
- Industry Wide Standard is enabler. Several standards should be avoided
 - Standards development should be **Quick, Open** and **Inclusive**
 - UPF 1.0 is fulfilling this requirement
- In PM target should be correct by construction, but in case there are escapes, bugs should be visible during verification.

Functional Bug Timing Bug PM Bug

